COMPUTER SCIENCE TRIPOS Part IA

Tuesday 6 June 2000 1.30 to 4.30

Paper 2

Answer the question in Section A, **one** *question from each of Sections B and C, and* **two** *questions from Section D.*

Submit the answers in five **separate** *bundles, each with its own cover sheet. On each cover sheet, write the numbers of* **all** *attempted questions, and circle the number of the question attached.*

Write on **one** *side of the paper only.*

SECTION A

1 Multi-part question

Answer all five parts.

(*a*) Prove that there are no integer solutions to $x^5 - 3x^2 + 2x - 1 = 0$. [4 marks]

(*b*) Draw a picture of a *deterministic* finite automaton which accepts the language of strings matching a^*ba. [4 marks]

(*c*) Describe the operation of the Unix shell with reference to the process management system calls it makes use of. You might like to use pseudo-code or a diagram to aid your description. [4 marks]

(*d*) What is the purpose of a formal specification language such as Z? [4 marks]

(*e*) Describe ML's datatype declaration. Show an example of a function declaration that uses pattern matching on possible values of the data type. [4 marks]

SECTION B

2 Digital Electronics

What is the maximum number of terms there can be in a minimal sum of products form of a function of n boolean variables? [2 marks]

Consider a two-bit multiplier with inputs x_1, x_0, y_1, y_0 and outputs z_3, z_2, z_1, z_0 such that

$$Z = Y \times X$$

where Z, Y, X are the positive integers represented by $z_3z_2z_1z_0$, y_1y_0 and x_1x_0 using the obvious representation.

Find a minimal sum of products expression for each of z_3, z_2, z_1 and z_0. [10 marks]

Comment on the complexity of building an eight-bit multiplier using a minimal sum of products form. [3 marks]

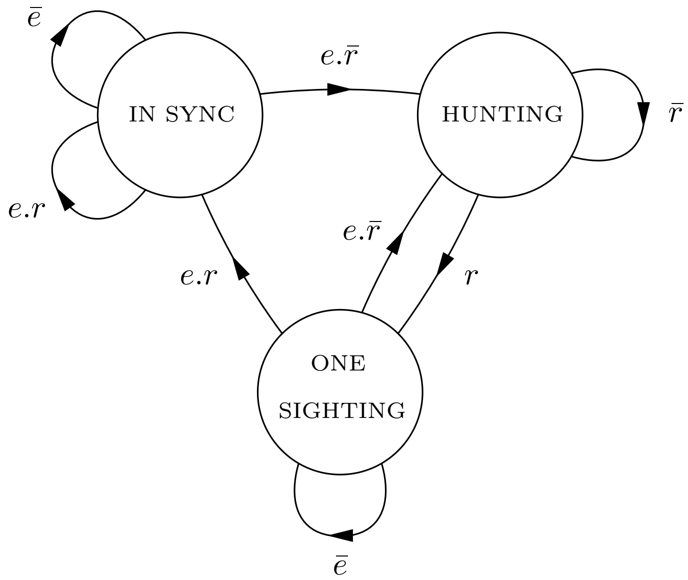
Describe another way of building an eight-bit multiplier. [5 marks]

3 Digital Electronics

You are required to build a circuit whose inputs are a data input D and a clock C. The data input D is used to pass a stream of bits into the circuit. Every 64 bits, an 8-bit synchronisation pattern 01100110 appears in the stream, followed by 56 bits of changing information.

(*a*) Design a combinational circuit incorporated with an 8-bit shift register that recognises the synchronisation pattern and asserts a signal r for 1-bit time whenever the pattern appears. [5 marks]

(*b*) The pattern 01100110 may of course appear in the changing information bits. Thus we must have some means of remembering if we are in sync so that we can expect the 01100110. Let us use the following state diagram, where e (expected) will be true whenever we expect to see r true.



Explain what each of the states is for and implement the finite state machine described in the diagram, including the equation of s which is true while the machine remains in synchronisation. [10 marks]

(*c*) Explain briefly how the signal e might be produced. [2 marks]

(*d*) Another output, the byte clock b, is to have a low to high transition every eight bits, with one such transition occurring when an expected synchronisation pattern appears in the shift register (and then eight bits later, etc.). Explain how this signal might be produced. [3 marks]

SECTION C

4 Probability

An ordinary fluorescent light tube exhibits a lack of memory property in that its life expectancy does not depend on how long it has been working. A typical tube may be expected to work for another 5040 hours no matter how long it has been working so far.

If a room contains eight such tubes and all are working, one may expect the first failure after 630 hours (5040/8). If the dud tube is *not* replaced, after how many more hours may one expect the second failure and (again assuming no replacement) after how many more may one expect the third failure? [2 marks]

Consider a meeting room which is equipped with four light fittings, each equipped with two such tubes. The management has decided that the room lighting is acceptable provided at least one tube in each pair is working. As soon as a second tube fails in any one fitting, a maintenance crew replaces *all* dud tubes in the room. Starting with eight working tubes, the crew may be called out as early as the second failure or as late as the fifth failure.

Let X be a random variable whose value r is the number of dud tubes at the moment the maintenance crew is called out. Clearly $\mathrm{P}(X = 0) = \mathrm{P}(X = 1) = 0$. Determine the values of $\mathrm{P}(X = 2)$, $\mathrm{P}(X = 3)$, $\mathrm{P}(X = 4)$ and $\mathrm{P}(X = 5)$. Express all four results as fractions. It may be assumed that all fittings are permanently switched on and that tubes fail independently. [12 marks]

What is the expectation, $\mathrm{E}(X)$? [4 marks]

The management rounds the value of $\mathrm{E}(X)$ down to the nearest integer and uses the derived value for estimating the number of tubes that have to fail between successive call-outs of the maintenance crew and the time interval between such call-outs. What is this time interval in hours? [2 marks]

5 Probability

An arbitrary value is loaded into an n-bit register. Let u_n be the probability that there are no instances of two (or more) adjacent bits being 0s.

A hardware designer suspects (correctly) that u_n is related to u_{n-1} and u_{n-2}. Write down the second-order difference equation which relates these terms. [8 marks]

Justify the use of $u_0 = u_1 = 1$ as initial conditions. [2 marks]

Solve the difference equation using these initial conditions. [10 marks]

SECTION D

6 Professional Practice and Ethics

What moral obligations are incurred through becoming a member of a professional body such as the British Computer Society, and how would you justify these moral obligations? [20 marks]

7 Regular Languages and Finite Automata

For each kind of regular expression over an alphabet Σ, define the language $L(\mathbf{r})$ of strings matching a regular expression $\mathbf{r}$ of that kind. [4 marks]

Define the language $L(M)$ accepted by a deterministic finite automaton M. [2 marks]

Prove that for every deterministic finite automaton M with alphabet of input symbols Σ it is possible to construct a regular expression $\mathbf{r}$ over Σ satisfying $L(\mathbf{r}) = L(M)$. [10 marks]

Illustrate your proof by constructing such an $\mathbf{r}$ for the deterministic finite automaton with state set $\{0, 1, 2\}$, alphabet of input symbols $\{a, b\}$, initial state 0, accepting states 1 and 2, and next-state function

$$\begin{array}{lll} (0,a) \mapsto 2, & (1,a) \mapsto 1, & (2,a) \mapsto 0, \\ (0,b) \mapsto 1, & (1,b) \mapsto 0, & (2,b) \mapsto 2. \end{array}$$

[4 marks]

8 Software Engineering I

One means of improving system reliability is to have three or more replicated systems and act on their majority output. Give *two* examples of failure that can be stopped by the mechanism, and *two* which cannot. At least one of each type should be illustrated by an actual case history or application. [12 marks]

An engineer attempts to improve the reliability of such a system further by multiversion programming – by having three separate systems coded by different teams and possibly in different languages. Discuss what might still go wrong. [8 marks]

9 Software Engineering II

Consider this program over integer variables:

```
k := K;
x := X;
z := 1;
while k <> 0 do
  begin
    k := k-1;
    z := z*x
  end
```

Given that the loop invariant is $z \times x^k = X^K$, show that executing this program stores the value of X^K in the variable z. [5 marks]

It is proposed to insert the following code just before the assignment `k := k-1`:

```
while even(k) do
  begin
    k := k/2;
    x := x*x
  end
```

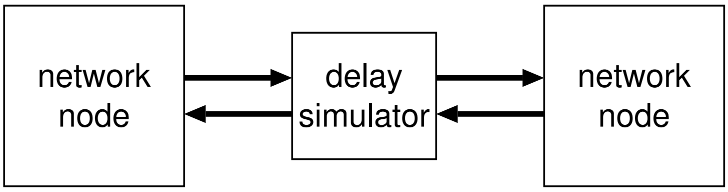
State the loop invariant of this inner loop and show that the modified program still stores the value of X^K in z. [7 marks]

Briefly describe formal specification languages, top–down design and fault avoidance techniques, indicating their respective roles in a software development project. [8 marks]

10 Structured Hardware Design

Some networking researchers wish to investigate the behaviour of a networking protocol when it is operating over long distance (high latency) links. To do this, they intend to build a *network delay simulator*, which they will use to interconnect a pair of network nodes. Operating concurrently on each link direction, the device will receive the data stream, delay it, then transmit it onwards to the other node.

The network uses a serial link operating at one gigabit per second, and the researchers require to be able to vary the delay such as to simulate links of between 1 and 5000 kilometres in length.



How much buffer memory is required to implement the device? [3 marks]

How can the data on the high-speed serial links be converted to a more manageable form? [4 marks]

Outline a design for the delay simulator, and hence address the following points:

- How many banks of memory does your design require, and what type(s) will be used?
- How will the control logic function, and what technology will it be built using?
- How will the delay inserted by the device be adjusted?

[13 marks]

END OF PAPER