## COMPUTER SCIENCE TRIPOS Part IA - 2023 - Paper 2

## 1 Digital Electronics (ijw24)

(a) Simplify the following Boolean function into both sum of products and product of sums forms, taking into account the don't care terms $A . B$ and A.C

$$
F(A, B, C, D)=\bar{A} \cdot B \cdot \bar{C}+A \cdot \bar{B} \cdot \bar{C}+\bar{A} \cdot \bar{B} \cdot D+\bar{A} \cdot C \cdot \bar{D}
$$

(b) Using a Karnaugh Map, simplify the following Boolean function into sum of products form
$G(A, B, C, D)=(\bar{A}+\bar{B}+C) \cdot(B+C+\bar{D}) \cdot(A+\bar{B}+D) \cdot(\bar{A}+B+\bar{D}) \cdot(\bar{B}+C+D)$
[3 marks]
(c) For the following circuit, assume that all the logic gates have an equal value of non-zero propagation delay and that $X=0$ and $Y=0$

(i) With the aid of a timing diagram, show that a static hazard is present at output $P$ when input $Z$ changes from 0 to 1 .
(ii) With the assistance of a Karnaugh Map, show how the static hazard identified in Part $(c)(i)$ can be eliminated.
(d) (i) Show how the following Boolean function may be implemented using an 8:1 multiplexer. Use variable $X$ as the most significant bit of the multiplexer selector inputs

$$
M(X, Y, Z)=\bar{X} \cdot \bar{Y} \cdot Z+\bar{X} \cdot Y \cdot Z+X \cdot \bar{Y} \cdot \bar{Z}+X \cdot \bar{Y} \cdot Z
$$

(ii) Show how the function in Part $(d)(i)$ may alternatively be implemented using a 2:1 multiplexer and a NOT gate. Assume that complemented input variables are not available.

