## COMPUTER SCIENCE TRIPOS Part IA - 2022 - Paper 2

## 2 Digital Electronics (ijw24)

(a) A (fictional) edge-triggered $U V$ flip-flop has inputs $U$ and $V$ and output $Q$. Its state-transition table is given by:

| Current state $(Q)$ | Next state $\left(Q^{\prime}\right)$ |  |  |  |  |
| :---: | ---: | :---: | :---: | :---: | :---: |
|  | $U V=$ | 00 | 01 | 10 | 11 |
| 0 | 0 | 1 | 0 | 1 |  |
| 1 | 0 | 0 | 0 | 1 |  |

(i) Draw the state-transition diagram for the $Q$ output.
(ii) For an implementation based on a D-type flip-flop, determine the simplified Boolean equation in sum-of-products form for the next-state ( $Q^{\prime}$ ) logic.
[2 marks]
(b) Consider the following state machine:

(i) Assuming that the machine starts in state $S_{0}$ and that the input data sequence at input $(X)$ is appropriately synchronised with the state machine clock, determine the next-state and output sequences for the input sequence 0101011011011. What operation does the machine perform? [5 marks]
(ii) For an implementation based on two D-type flip-flops (labelled $A$ and $B$ ), determine simplified Boolean expressions for the next-state and output combinational logic, assuming the state assignment $S_{0}=00, S_{1}=01$ and $S_{2}=10$ is used, where a state is labelled $Q_{A} Q_{B}$ in terms of the flip-flop outputs.
(iii) For an alternative one-hot implementation based on D-type flip-flops, determine expressions for the next-state and output logic.
[4 marks]
(iv) What feature, inherent in the proposed state-machine design, may give rise to problems at the output $Y$ ? How might this be addressed?
[2 marks]

