

13 System-on-Chip Design (DJG)

- (a) The police services of all European countries together decide to implement a new datacentre to host a shared database that holds human DNA fingerprints. The main operation that requires high-performance will be lookup by string matching.

For each of the following design considerations, write notes on the suitability of custom hardware accelerators in general and for the specific police DNA application.

- (i) The type of arithmetic and logic likely to be needed. [2 marks]
- (ii) The memory bandwidth and overall topology. [2 marks]
- (iii) The relative advantages of ASIC versus FPGA implementation. [3 marks]
- (iv) The likely energy and performance benefits. [2 marks]
- (b) An SSRAM is a static, synchronous random-access memory.
- (i) Draw a schematic symbol and/or describe the net-level connections to a typical SSRAM. [1 mark]
- (ii) Describe two ways in which an SSRAM may get instantiated in an RTL (Verilog or VHDL) design. [2 marks]
- (iii) What constraints does SSRAM have on its use in RTL? Give a conforming RTL fragment that increments one SSRAM location while obeying the constraints. [5 marks]
- (iv) In what stage of HLS do tools instantiate RAMs and how are constraints over port use overcome? [3 marks]