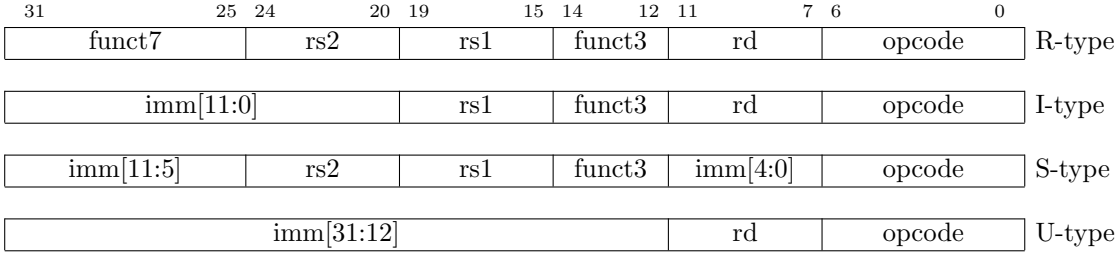
2 Computer Design (SWM)

The RISC-V base ISA instruction formats are reproduced below. Each immediate subfield is labelled with the bit position (imm[x]) in the immediate value being produced, rather than the bit position within the instruction's immediate field as is usually done.



(a) In assembler, what is an *immediate*? [2 marks]

(b) Give examples of *load*, *branch* and *arithmetic* instructions in assembler that use an immediate. Note that it is not critical for the RISC-V assembler syntax to be perfect, but for each instruction please explain your answer. [3 marks]

(c) For a pipelined processor implementation, why is it an acceptable design choice for the bit position of immediates to vary between instruction formats? [2 marks]

(d) For a pipelined processor implementation, why is it advantageous to have the source registers in the same bit position independent of the instruction format? [2 marks]

(e) Why can there be many more register-to-register instructions with no immediates than instructions with immediates? [3 marks]

(f) For a pipelined implementation of the RISC-V ISA, the sequential instruction execution model needs to be preserved. Cases where the pipelined implementation might deviate from this sequential model are often referred to as *hazards*. For a simple pipelined implementation, what hazards might exist and how might they be resolved? [8 marks]