12 System-on-Chip Design (DJG)

A hardware FIFO is a type of memory component. It has two ports, one for reading and one for writing, and implements the first-in/first-out queuing discipline.

(*a*) Why is flow control important when using FIFOs and what net-level signals must a hardware FIFO accept and generate for proper handshaking? [3 marks]

(*b*) Give a suitable signature of such a FIFO component in either a Register Transfer or Transactional Level Modelling language (RTL or TLM). Explain in detail how the handshaking works with your signature. Comment on how it would differ for the other signature.
Note: the signature of a component is its interface type, where method bodies or implementation logic are missing, such as `(input [6:0] foo, output bar)` in Verilog. [6 marks]

(*c*) In an embedded system, a FIFO is to be used for passing messages, in one direction, between a pair of processors that share no memory but which each have memory-mapped access to one of the FIFO's ports. An interrupt-driven device driver would offer no advantage in the target application. Using assembler, C or pseudocode, give either the read or write methods of a polling device driver and explain how the other would differ. [5 marks]

(*d*) An alternative approach for passing data between the pair of processors is to use shared memory. You are asked to predict the performance and energy use of the two designs in advance of making the hardware. Discuss the role a TLM model might have and whether there is a better alternative model or technique. [6 marks]