

COMPUTER SCIENCE TRIPOS Part IB – 2017 – Paper 5

3 Computer Design (TMJ)

A shared-memory multicore processor contains three cores, each with a private L1 cache connected to a bus along with a shared L2 cache. Coherence is maintained through a basic MSI cache coherence protocol.

(a) What is a shared-memory multicore processor? [2 marks]

(b) Contrast the memory hierarchy described above against one containing multiple private L2 caches (with the same total L2 cache space). [6 marks]

(c) Describe whether each of the following scenarios represents a valid combination of coherence states across the L1 caches for data at a particular memory address. For example, [M, M, M] represents the data being in state M in each of the three L1 caches in the processor.

(i) [M, M, M]

(ii) [S, S, S]

(iii) [I, I, I]

(iv) [M, S, I]

[8 marks]

(d) Describe the disadvantages of the basic MSI protocol in each of the following scenarios.

(i) A core modifies private data that it has already read.

(ii) A core reads data that is already in another core's L1 cache.

[4 marks]