1 Computer Design (SWM)

(a) Write one or more lines of SystemVerilog that correspond to a complete module for each of the following circuits. Aim for simplicity and explain any subtleties of your implementation.

(i) a[0]
a[1]
a[2]
a[3]
a[4]
a[5]
a[6] → b

(ii) d  4
    e  4
    +  full adder
    5  f

(iii) 4'd1
      g  4
      full adder 4
      clear 4
      0  r
      1  h
      load 4
      clk

[4 marks]
[4 marks]
[4 marks]
(b) Consider the following SystemVerilog module:

```systemverilog
module gcd(
    input logic clk,
    input logic rst,
    input logic start,
    input logic [15:0] Ain,
    input logic [15:0] Bin,
    output logic [15:0] answer,
    output logic done
);

logic [15:0] a, b;
always_ff @(posedge clk or posedge rst)
    if(rst)
        begin
            a <= 0;
            b <= 0;
            answer <= 0;
            done <= 0;
        end
    else if(start)
        begin
            a <= Ain;
            b <= Bin;
            done <= 1'b0;
        end
    else if(b==0)
        begin
            answer <= a;
            done <= 1'b1;
        end
    else if(a>b)
        a <= a-b;
    else
        b <= b-a;
endmodule
```

(i) For inputs Ain=21 and Bin=15, complete the following state transition table (where X means undefined or unknown values): [6 marks]

<table>
<thead>
<tr>
<th>Ain</th>
<th>Bin</th>
<th>start</th>
<th>a</th>
<th>b</th>
<th>a'</th>
<th>b'</th>
<th>done'</th>
<th>answer'</th>
</tr>
</thead>
<tbody>
<tr>
<td>21</td>
<td>15</td>
<td>1</td>
<td>X</td>
<td>X</td>
<td>21</td>
<td>15</td>
<td>0</td>
<td>X</td>
</tr>
<tr>
<td>21</td>
<td>15</td>
<td>0</td>
<td>21</td>
<td>15</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(ii) What values of Ain and Bin will cause the module to fail to terminate (i.e. done will never go high)? [2 marks]