1 Digital Electronics (IJW)

(a) Consider a 4-input Boolean function that outputs a binary 1 whenever an odd number of its inputs are binary 1.

(i) Using Boolean logic or otherwise, show how the above function can be implemented using only 2-input XOR gates.

(ii) Show how the above function may alternatively be implemented using one 4-input decoder, and a minimum number of 4-input NOR and 4-input NAND gates.

[7 marks]

(b) Consider the following Boolean expression

\[ F = \overline{B}.\overline{C} + \overline{A}.B.C + A.C.D \]

(i) Show that \( F \) can be represented by the following Product of Sums (POS) form

\[ F = (\overline{B} + C).(\overline{A} + \overline{C} + \overline{D}).(A + B + \overline{C}) \]

(ii) Show how \( F \) can be implemented in a 2-level form using OR gates followed by an AND gate. Remember to indicate any NOT gates required, since only uncomplemented input variables are available.

[5 marks]

(c) Consider your implementation in part (b)(ii).

(i) Assume that the gates have finite propagation delay. Describe in detail what happens at the output \( F \) when the inputs \( \{A, B, C, D\} \) change from \( \{1, 1, 0, 1\} \) to \( \{1, 1, 1, 1\} \).

(ii) Using a Karnaugh map or otherwise, determine the other single input variable change that will give rise to a similar problem to that observed in part (c)(i).

(iii) Using a Karnaugh map or otherwise, determine a modified POS expression for \( F \) that will eliminate the problems observed in parts (c)(i) and (c)(ii).

[8 marks]