

COMPUTER SCIENCE TRIPOS Part IB – 2014 – Paper 5

3 Computer Design (SWM)

- (a) What is a data cache and how does it differ from an instruction cache? [4 marks]
- (b) What statistical properties of memory access do caches exploit to deliver improved performance? [4 marks]
- (c) What impact will an operating-system-managed context switch have on cache hit rate? Justify your answer. [4 marks]
- (d) Modern desktop and server processors support simultaneous multithreading (also called *hyperthreading*). When will there be a performance benefit in scheduling two non-interactive applications on the same hyperthreaded processor core so that they run in parallel rather than running sequentially, one job one after the other? [4 marks]
- (e) For level-1 data caches using a snoopy cache coherency protocol, is a write-back or a write-through policy more likely to be used? [4 marks]