1 Digital Electronics (IJW)

(a) A combinational logic circuit takes a 4-bit unsigned binary integer number at its inputs labelled $D_3$, $D_2$, $D_1$ and $D_0$, where $D_3$ is the most significant bit. For decimal input 1, 2, 3, 5, 7, 11 and 13, the output $S$ is to be at logic 1, and it is to be at logic 0 otherwise.

(i) Write down the truth table for the required combinational logic function.

(ii) Using a Karnaugh map, determine the simplified Boolean expression for the output $S$ in terms of the inputs $D_3$ to $D_0$ in a minimum sum-of-products form.

(iii) Describe what is meant by an essential term in a Karnaugh map. Write down the essential terms for the Karnaugh map in (ii).

(iv) Using a Karnaugh map, this time determine the required simplified Boolean expression for the output $S$ in a minimum product-of-sums form.

[10 marks]

(b) Provide a circuit diagram which implements the following Boolean function using only NAND gates

$$F = (A + \overline{D}).(B + C + \overline{D}).(A + \overline{B} + \overline{C})$$

that has the don’t care states: $A.B.C.D$, $A.B.\overline{C}.D$, $A.B.C.D$ and $A.B.C.\overline{D}$

[4 marks]

(c) Show that

$$(X + Y).(X + Z) = X + Y.Z$$
$$(X + Y).(\overline{X} + Z) = X.Z + \overline{X}.Y$$

Using these results or otherwise, simplify the following expression

$$P = (A + B + \overline{C}).(A + B + D).(A + B + E).(A + \overline{D} + E).(\overline{A} + C)$$

[6 marks]