COMPUTER SCIENCE TRIPOS Part IA – 2013 – Paper 2

2 Digital Electronics (IJW)

(*a*) With the use of appropriate diagrams, briefly explain the operation of Moore and Mealy finite state machines, paying particular regard to their differences.

[6 marks]

(*b*) A serial data line carries binary data to a system with input X. The system is required to detect a sequence $0\,1\,0$ in the data and give an output $Y = 1$ at the end of the sequence. Only non-overlapping sequences should be detected in the data. For example, the output Y should only be 1 for the 0 underlined in the input sequence $\ldots\, 1\,0\,1\,\underline{0}\,1\,0\,1\,\ldots$.

Draw the state diagram for the system and state the minimum number of D-type bistables that are required to implement this finite state machine.

[6 marks]

(*c*) A finite state machine (FSM) has the following sequence of states at the outputs of its D-type state registers, Q_A , Q_B and Q_C :

Q_A	Q_B	Q_C
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
0	0	0
⋮	⋮	⋮

if the state registers are initialised to state $0\,0\,0$, or

Q_A	Q_B	Q_C
1	1	1
1	1	0
1	0	1
1	1	1
⋮	⋮	⋮

if the state registers are initialised to state $1\,1\,1$.

Determine the next state combinational logic required to implement this FSM.

[8 marks]