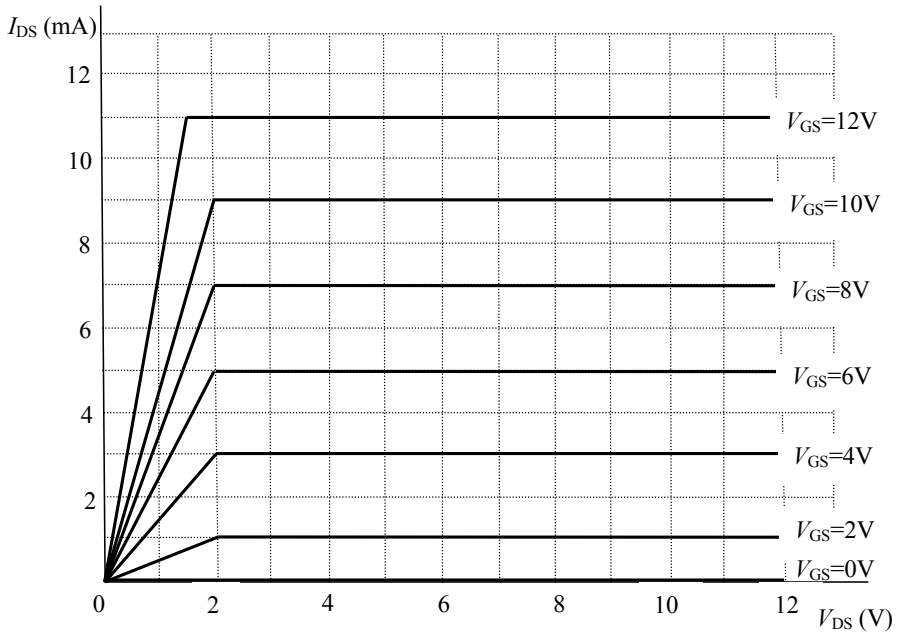
COMPUTER SCIENCE TRIPOS Part IA – 2012 – Paper 2

2 Digital Electronics (IJW)

(*a*) With the aid of appropriate diagrams, show how the Source–Drain current that flows in a p-channel MOSFET is controlled by the applied Gate–Source voltage. [4 marks]

(*b*) (*i*) Draw the circuit diagram of a NOT gate that comprises an n-channel MOSFET and a resistor R. [2 marks]

(*ii*) For the NOT gate in (*b*)(*i*), plot the relationship between the input voltage, V_{in} and the output voltage, V_{out}. Assume that the power supply voltage $V_{\text{DD}} = 12$ V, $R = 1$ kΩ, and that the MOSFET has the characteristics given in the following figure. [4 marks]



(*c*) For the NOT gate in (*b*), calculate the power dissipated by the entire gate and that by resistor R alone, when $V_{\text{in}} = 12$ V. [4 marks]

(*d*) The stray capacitance present at the output of the NOT gate in (*b*) can be represented by a capacitor, $C = 100$ nF connected between the gate output and 0 V. Also assume that the MOSFET has an ON resistance $R_{\text{on}} = 100$ Ω. The input signal, V_{in}, is a 1 kHz square wave with minimum and maximum amplitudes of 0 V and 12 V respectively.

(*i*) Sketch the output signal waveform, V_{out}, of the NOT gate being sure to include indicative rise and fall times and voltage levels. [4 marks]

(*ii*) How could the rise-time of V_{out} be reduced and what would be the impact of your proposed solution on the power dissipation of the circuit?

[2 marks]