Computer Design

Consider the following UltraRISC processor which has just one instruction (so there is no opcode), with one operand (an address).

```verilog
module UltraRISC();
    logic [7:0] mem[31:0]; // memory
    logic [7:0] pc; // program counter
    logic [7:0] ir; // instruction register
    logic [7:0] acc; // accumulator
    logic step;
    logic clk;
    logic [7:0] next_pc, next_ir;
    logic [8:0] next_acc;
    logic borrow;
parameter Lt=16, Lx=17, Ly=18, Lz=19, Lstop=31;
initial begin
    clk <= 1; pc <= 0; step <= 0; acc <= 0;
    // Code Data
    mem[ 0] <= Lt; mem[Lt] <= 13; // holds T
    mem[ 1] <= Lt; mem[Lx] <= 13; // holds X
    mem[ 2] <= Lt; mem[Ly] <= 7; // holds Y
    mem[ 3] <= Lx; mem[Lz] <= 3; // holds Z
    mem[ 4] <= Lx; mem[Lstop] <= 0;
    mem[ 5] <= Ly;
    mem[ 6] <= Lt;
    mem[ 7] <= Lt;
    mem[ 8] <= Lx;
    mem[ 9] <= Lt;
    mem[10] <= Lt;
    mem[11] <= Lt;
    mem[12] <= Lz;
    mem[13] <= Lx;
    mem[14] <= Lstop;
    mem[15] <= 0;
end // initial begin
always #5 clk <= !clk;
```

[continued. . .]
always_comb
    if(step==0) begin
        next_ir = mem[pc];
        next_acc = acc;
        next_pc = pc+1;
    end else begin
        next_ir = ir;
        next_acc = mem[ir]-acc;
        borrow = next_acc[8];
        next_pc = pc+borrow;
    end

always_ff @(posedge clk) begin
    step <= !step;
    ir <= next_ir;
    pc <= next_pc;
    acc <= next_acc;
    if(step) mem[ir] <= next_acc;
    if(ir==Lstop) begin
        $display("result = %d, finished",acc);
        $finish;
    end
end
endmodule

(a) What is the CPI (cycles per instruction) for this processor? [3 marks]

(b) What function does the one instruction perform? [5 marks]

(c) What result is produced when the program held in mem is executed? Explain your answer. [10 marks]

(d) How does the code density compare with the MIPS32 ISA? [2 marks]