Computer Design

(a) Given a positive reset signal, how is an asynchronous reset described in Verilog? [2 marks]

(b) For each of the following six always blocks, what sequence or error will be produced? You should assume that registers are reset to zero at the start (as they are for FPGAs) and that clk is a clock. [3 marks each]

```verilog
reg [2:0] counterA, counterB, counterC, counterD, counterE, counterF;

always @(posedge clk)
begin
    counterA <= counterA+1;
    if(counterA==5) counterA <= 1;
end

always @(posedge clk)
begin
    if(counterB==5) counterB <= 1;
    counterB <= counterB+1;
end

always @(posedge clk)
begin
    if(counterC==5) counterC = 1;
    counterC = counterC+1;
end

always @(posedge clk)
begin
    counterE <= (counterD==5) ? 1 : counterD;
end

always @(posedge clk)
begin
    if(counterF==5) counterF <= 1;
    counterF <= counterF+1;
end
```