ECAD

(a) In the Verilog hardware description language, what is the difference between continuous, blocking and non-blocking assignments? [6 marks]

(b) What is the labelled circuit diagram which corresponds to the following snippet of Verilog? [3 marks]

```verilog
reg [1:0] s;
wire t;
always @(posedge clk) s <= {s[0], t};
```

(c) A naïve programmer has written the following Verilog module to sort two 4-bit values a and b such that a<b.

```verilog
module sort2(clk,a,b);
    input clk;
    input [4:0] a;
    input [4:0] b;
    wire [4:0] t;
    always @(clk) begin
        if(a > b) begin
            t <= a;
            a <= b;
            b <= t;
        end
    end
endmodule
```

(i) What is wrong with the code above? [6 marks]

(ii) How would you correct this module so that it takes two values as input and outputs the sorted values one clock cycle later? [5 marks]