2005 Paper 7 Question 1

Comparative Architectures

(*a*) Most RISC architectures use a 32-bit fixed length instruction encoding. In contrast, Intel x86 and VAX use a variable length encoding, and the IA-64 uses 128-bit instruction "bundles". Compare and contrast these different instruction encodings, with particular reference to their ease (or otherwise) to decode in a super-scalar implementation, and the "code density" they achieve. [10 marks]

(*b*) Discuss the pros and cons of architectures with a 64-bit word size *versus* those with a 32-bit word size. Which applications are likely to benefit most? [4 marks]

(*c*) If you were a processor architect targeting embedded applications where memory is a scarce resource, how might you design a RISC-like instruction set that will achieve efficient use of memory? [6 marks]