Computer Design

The ARM processor allows the second operand to be shifted by an arbitrary amount. In order to improve the performance, a six-stage pipeline is proposed with the following stages:

| instruction fetch | decode and register fetch | shift operand 2 | execute | memory access | register write back |

(a) What are control hazards and how could they be resolved in the above pipeline? [4 marks]

(b) What are data hazards and how could they be resolved in the above pipeline? [4 marks]

(c) What are feed-forward paths and where could they be added to the above pipeline to improve performance? [6 marks]

(d) Why might a branch instruction result in pipeline bubbles and how many bubbles will appear in the above pipeline as a result of taking a branch instruction? [6 marks]