Consider the following mysterious Verilog module.

```verilog
module mystery(c,r,a,s);
    input c,r,a;
    output [2:0] s;
    reg [2:0] s;
    always @(posedge c or posedge r)
        if(r)
            s<=0;
        else begin
            if(a && (s<7)) s<=s+1;
            else if(!a && (s>0)) s<=s-1;
        end
    endmodule
```

(a) How many flip-flops will be required to implement the mystery module, and how will signals \( c \) and \( r \) be connected to these flip-flops? [5 marks]

(b) What is the state transition diagram for this mystery module? [5 marks]

(c) If this module were synthesised to the minimum sum of products form, what would the equations be for next state bits \( s[0] \), \( s[1] \) and \( s[2] \)? [10 marks]