Digital Electronics

(a) An $n$-bit decoder is a combinational circuit with $n$ inputs and $2^n$ outputs. For each possible assignment of values to inputs there is a corresponding output which is set to “1” when and only when that assignment is made to the inputs. Give a design for a 3-bit decoder. [4 marks]

(b) Ignoring inverters, how many gates are required for your design? How many are required for an $n$-bit decoder? [2 marks]

(c) An $n$-bit priority encoder has $2^n - 1$ inputs and $n$ outputs. The inputs $x_1, x_2 \ldots x_{2^n-1}$ are ordered in priority with $x_j$ having higher priority than $x_i$ if $j > i$. The outputs $a_{n-1}, a_{n-2} \ldots a_0$, interpreted as an unsigned integer, denote the highest priority input asserted high. Give a design for a 3-bit priority encoder. [6 marks]

(d) Give two designs for a combinational circuit which has $K$ ordered inputs and $K$ corresponding outputs where the only output asserted (if any) is the one corresponding to the asserted input with the highest priority. [6 marks]

(e) Which design is better, and why? [2 marks]