2002 Paper 10 Question 1

Digital Electronics

You are to design a sequencer with the following properties.

- There are four inputs: `reset`, s_0, s_1, s_2.

- There are three outputs: t_0, t_1, t_2.

You may assume that there is a clock.

Once the system is reset, the signals s_0, s_1, s_2 may be asserted in any order. However, the t_i may be asserted only if all of the $s_j, j \leqslant i$ have been asserted since the last reset. You may assume that once an s_i is asserted it remains so until the reset is applied.

(a) Draw a state diagram for the system. [6 marks]

(b) Provide a state transition table for the system. [4 marks]

(c) Provide equations for next state control and outputs for an implementation. [6 marks]

(d) Suppose that the s_i did not remain asserted until system reset. How would you modify the implementation? [4 marks]