APPENDIX B

OVERALL TECHNOLOGY CHARACTERISTICS TABLES

Table B–1 Overall Roadmap Technology Characteristics

YEAR OF FIRST PRODUCT SHIPMENT	*1997*	*1999*	*2001*	*2003*	*2006*	*2009*	*2012*
TECHNOLOGY GENERATIONS DENSE LINES (DRAM HALF-PITCH) (nm)	*250*	*180*	*150*	*130*	*100*	*70*	*50*
ISOLATED LINES (MPU GATES) (nm)	*200*	*140*	*120*	*100*	*70*	*50*	*35*
Memory							
Generation @ samples/introduction	256M	1G	*	4G	16G	64G	256G
Generation @ production ramp	64M	256M	1G	1G	4G	16G	64G
Bits/cm2 @ sample/introduction	96M	270M	380M*	770M	2.2B	6.1B	17B
"Affordable" cost/bit @ (packaged—microcents) @ samples/introduction	120	60	30*	15	5.3	1.9	0.66
Logic (High-Volume—Microprocessor)†							
Logic transistors/cm^2 (packed, including on-chip SRAM)	3.7M	6.2M	10M	18M	39M	84M	180M
"Affordable" cost/transistor @ (packaged-microcents)	3000	1735	1000	580	255	110	50
Logic (Low-Volume—ASIC)‡							
Usable transistors/cm^2 (auto layout)	8M	14M	16M	24M	40M	64M	100M
Nonrecurring engineering cost/usable transistor (microcents)	0.05 50	0.025 25	0.02 20	0.015 15	0.01 10	0.005 5	0.0025 2.5
Number of Chip I/Os							
Chip-to-package (pads) (high-performance)	1450	2000	2400	3000	4000	5400	7300
Chip-to-package (pads) (cost-performance)	800	975	1195	1460	1970	2655	3585
Number of Package Pins/Balls							
Microprocessor/controller (cost-performance)	600	810	900	1100	1500	2000	2700
ASIC (high-performance)	1100	1500	1800	2200	3000	4100	5500
Package cost (cents/pin) (cost-performance)	1.40–2.80	1.25–2.50	1.15–2.30	1.05–2.05	0.90–1.75	0.75–1.50	0.65–1.30
Chip Frequency (MHz)							
On-chip local clock (high-performance)	750	1250	1500	2100	3500	6000	10000
On-chip, across-chip clock (high-performance)	750	1200	1400	1600	2000	2500	3000
On-chip, across-chip clock (high-performance ASIC)	300	500	600	700	900	1200	1500
On-chip, across-chip clock (cost-performance)	400	600	700	800	1100	1400	1800

** Generation is for trend purposes only*
† Year 1 data will be less dense than subsequent shrinks
‡ Refers to high-performance, leading-edge, embedded-array ASICs

Table B1 Overall Roadmap Technology Characteristics (Continued)

YEAR OF FIRST PRODUCT SHIPMENT	*1997*	*1999*	*2001*	*2003*	*2006*	*2009*	*2012*
TECHNOLOGY GENERATIONS DENSE LINES (DRAM HALF-PITCH) (nm)	*250*	*180*	*150*	*130*	*100*	*70*	*50*
ISOLATED LINES (MPU GATES) (nm)	*200*	*140*	*120*	*100*	*70*	*50*	*35*
Chip Frequency (MHz) (continued)							
Chip-to-board (off-chip) speed (high-performance, reduced-width, multiplexed bus)	750	1200	1400	1600	2000	2500	3000
Chip-to-board (off-chip) speed (high-performance, peripheral buses)	250	480	785	885	1035	1285	1540
Chip Size (mm^2)							
DRAM	280	400	445*	560	790	1120	1580
Microprocessor	300	340	385	430	520	620	750
ASIC [max litho field area]	480	800	850	900	1000	1100	1300
Lithographic Field Size (mm^2)	22 × 22 484	25 × 32 800	25 × 34 850	25 × 36 900	25 × 40 1000	25 × 44 1100	25 × 52 1300
Maximum Number Wiring Levels	6	6–7	7	7	7–8	8–9	9
DRAM *1st Year Electrical D_O @ 60% Yield/* *3rd Year @ 80% Yield (d/m^2)*	2080 /1390	1455 /985	1310* /875*	1040 /695	735 /490	520 /350	370 /250
MPU *1st Year Electrical D_O @ 60% Yield/* *3rd Year @ 80% Yield (d/m^2)*	1940 /1310	1710 /1150	1510* /1025*	1355 /910	1120 /760	940 /640	775 /525
ASIC *1st Year Electrical D_O @ 60% Yield* *(d/m^2)*	1210	725	685*	645	580	530	450
Minimum, mask count	22	22/24	23	24	24/26	26/28	28
Maximum substrate diameter (mm)							
Bulk or epitaxial or SOI***wafer	200	300	300	300	300	450	450
Power Supply Voltage (V)							
Minimum logic V_{dd} (V)	1.8–2.5	1.5–1.8	1.2–1.5	1.2–1.5	0.9–1.2	0.6–0.9	0.5–0.6
Maximum Power							
High-performance with heat sink (W)	70	90	110	130	160	170	175
Battery (W)—(Hand-held)	1.2	1.4	1.7	2.0	2.4	2.8	3.2
Design and Test							
Volume tester cost/pin ($K/pin) (high-performance)	10	10	10	10	10	10	10
Volume tester cost/pin ($K/pin) (cost-performance)	3	3	3	3	3	3	3

** Generation is for trend purposes only*
*** D_O—defect density*
**** Silicon On Insulator*
† *Year 1 data will be less dense than subsequent shrinks*
‡ *Refers to high-performance, leading-edge, embedded-array ASICs*

Table B–2 Multiple Year Intra-generation Data

YEAR OF FIRST PRODUCT SHIPMENT	*1997*	*1999*	*2001*	*2003*	*2006*	*2009*	*2012*
TECHNOLOGY GENERATIONS DENSE LINES (DRAM HALF-PITCH) (nm)	*250*	*180*	*150*	*130*	*100*	*70*	*50*
ISOLATED LINES (MPU GATES) (nm)	*200*	*140*	*120*	*100*	*70*	*50*	*35*
MATURING PRODUCT GENERATION LIFE CYCLE: CHARACTERISTICS PROJECTIONS							
Functions/Chip							
DRAM bits/chip—Years 1–6	267M	1.07G	1.7G*	4.29G	17.2G	68.7G	275G
Microprocessor total transistors/chip—Years 1–6	11M	21M	40M	76M	200M	520M	1.40B
Chip Size (mm^2)							
DRAM—Year 1	280	400	445*	560	790	1120	1580
DRAM—Year 3 (2^{nd} shrink)	170	240	270*	340	480	670	950
DRAM—Year 6 (2^{nd} cut-down—next gen.)	100	140	160*	200	280	390	550
Microprocessor—Year 1	300	340	385	430	520	620	750
Microprocessor—Year 3 (2^{nd} shrink)	180	205	230	260	310	370	450
Microprocessor—Year 6 (2^{nd} cut-down—next gen.)	110	125	140	150	180	220	260
Function Density (Functions/cm^2)							
DRAM Bits/cm^2—Year 1	96M	270M	380M*	770M	2.2B	6.1B	17B
DRAM—Year 3 (2^{nd} shrink)	160M	450M	640M*	1.3B	3.6B	10B	29B
DRAM—Year 6 (2^{nd} cut-down—next gen.)	270M	770M	1.1B*	2.2B	6.2B	18B	50M
Microprocessor total transistors/cm^2 (packed)—Year 1	3.7M	6.2M	10M	18M	39M	84M	180M
Microprocessor total transistors/cm^2 (packed)—Year 3 (2^{nd} shrink)	6.1M	10M	17M	29M	64M	140M	310M
Microprocessor total transistors/cm^2 (packed)—Year 6 (2^{nd} cut-down—next gen.)	10M	17M	29M	50M	110M	240M	530M
"Affordable" Packaged Unit Cost/Function (Microcents/Function)							
DRAM packaged unit cost/bit @ (microcents)—Year 1	120	60	30*	15	5.3	1.9	0.66
DRAM packaged unit cost/bit @ (microcents)—Year 3 (2^{nd} shrink)	36	18	9*	4.5	1.6	0.57	0.20
DRAM packaged unit cost/bit @ (microcents)—Year 6 (2^{nd} cut-down—next gen.)	6.0	3	1.5*	0.76	0.28	0.09	0.03
Microprocessor packaged unit cost/transistor @ (microcents)—Year 1	3000	1735	1000	580	255	110	49
Microprocessor packaged unit cost/transistor @ (microcents)—Year 3 (2^{nd} shrink)	910	525	305	175	75	34	15
Microprocessor packaged unit cost/transistor @ (microcents)—Year 6 (2^{nd} cut-down—next gen.)	290	167	97	56	24	11	4.7

** 1.7G Generation is for trend purposes only, and may not actually occur*

GLOSSARY OF OVERALL CHARACTERISTICS

Nominal Generational Scale

YEAR OF FIRST PRODUCT SHIPMENT (Inter-generation, Table B1 and B2)—Year in which the leading chip manufacturer supplies quantities of samples (10K–100K) of dynamic random access memories (DRAMs) that are manufactured with production tooling (Other technology family members, such as microprocessors (MPUs) of the same generation (same feature size], are now being introduced concurrently, and in some cases, ahead of the DRAM product.)

TECHNOLOGY GENERATIONS (Minimum Feature Size [nm])—Ground rules of process is governed by the smallest feature printed. The half-pitch of first-level interconnect dense lines is most representative of the DRAM technology level feature size. For logic, such as microprocessors (MPUs), gate length is most representative of the technology level.

MATURING PRODUCT GENERATION LIFE CYCLE: CHARACTERISTICS PROJECTIONS (Intra-Generation, Table B2)—Year 1 is the inter-generation first product shipment year. Manufacturing process and equipment technology improves continually within a given technology generation. Chip size "shrinks" occur annually to take advantage of the latest manufacturing process and equipment, which improve continually within a given technology generation.
Year 3 marks the completion of the second full production year of the product generation using the second shrink of the chip.
Year 6 (completion of 5th year of production) of a given product generation is actually manufactured using super-shrink (cut-down) product on the next technology-generation manufacturing line.

Characteristics Of Major Markets

Functions/Chip—The number of bits (DRAMs) or logic transistors (MPUs, application-specific integrated circuits [ASICs]) that can be cost-effectively manufactured on a single monolithic chip at the available technology level (Logic transistors include both SRAM and logic transistors.)

Chip Size (mm^2)—The typical area of the monolithic memory and logic chip that can be affordably manufactured at a given product and manufacturing technology node (Estimates are projected based upon historical data trends. Multi-chip-packaged memory and logic are not covered explicitly.)

"Affordable" Packaged Unit Cost/Function—Final cost in microcents of a tested and packaged chip divided by ***Functions/Chip***
Affordable costs are calculated from historical trends of affordable average selling prices [gross annual revenues of a specific product generation divided by the annual unit shipments] less an estimated gross profit margin of approximately 35% for DRAMs and 60% for MPUs. The affordability per function is a guideline of future market "tops-down" needs, and as such, was generated independently from the chip size and function density. Smaller chip sizes from technology and design improvements; increasing wafer diameters; decreasing equipment cost-of-ownership (CoO); increasing equipment overall equipment effectiveness; and reduced package and test costs, etc. are all needed to meet the affordability requirements.)

Functions/cm^2—The ***Functions/Chip*** on a single monolithic chip divided by the ***Chip Size***.

Memory

Generation @ Samples/Introduction—The anticipated bits/chip of the DRAM product generation introduced at a given manufacturing technology node

Generation @ Production Ramp—The anticipated bits/chip of the DRAM generation that is ramping into volume production at a given manufacturing technology node (This overlaps with the introduction of the next product generation.)

Bits/Chip—Nominal number of functional bits (after repair) on a single monolithic chip

Logic (High Volume—Microprocessor)

Microprocessor Total Transistors/Chip—Nominal number of all SRAM and logic transistors that are anticipated (based upon historical trends) to be on a single monolithic chip at a given technology node

Logic (Low Volume—ASIC)

Usable Transistors/cm^2 (Auto Layout)—Number of transistors per cm^2 designed by automated layout tools for highly differentiated applications produced in low volumes. High-performance, leading-edge, embedded-array ASICs include both on-chip array logic cells, as well as dense functional cells (MPU, I/O, SRAM, etc). Density calculations include the connected (useable) transistors of the array logic cells, in addition to all of the transistors in the dense functional cells.

NRE Cost/Transistor (Microcent)—Nonrecurring engineering cost in microcents (chip design, test design, masks, etc.) divided by the number of transistors/chip and amortized over the production volume.

Chip and Package—Physical and Electrical Attributes

Number Of Chip I/Os

Chip-to-package (pads)(high-performance)—Number of I/O pads of chip permanently connected to package plane for functional or test purposes and includes any direct chip-to-chip interconnections or direct chip attach connections to the board (Package plane is defined as any interconnect plane, leadframe, or other wiring technology inside a package, i.e., any wiring that is not on the chip or on the board.)

Number Of Package Pins/Balls

Microprocessor/controller cost-performance—Number of pins or solder balls presented by the package for connection to the board (This may be fewer than the number of chip-to-package pads because of internal power and ground planes on the package plane or multiple chips per package.)

ASIC (high-performance)—Same definition as microprocessor/controller

Package cost (cost-performance)—Cost of package envelope and external I/O connections (pins/balls) in cents/pin

Chip Frequency (MHz)

On-chip, local clock, high-performance—On-chip clock frequency of high-performance, lower volume microprocessors in localized portions of the chip

On-chip, across-chip clock, high-performance—On-chip clock frequency of high-performance, lower volume microprocessors for interconnect signals that run across the full width of the chip (Typically, this is lower than the localized clock performance due to capacitance loading of the long cross-chip interconnect.)

On-chip, across-chip ASIC clock, high-performance—Same as local clock high-performance

On-chip, across-chip, cost-performance—On-chip clock frequency of cost-performance high-volume microprocessors for interconnect signals that run across the full width of the chip

Chip-to-board (off-chip) speed (high-performance, reduced-width, mutiplexed bus)—Maximum signal I/O frequency to specialized board reduced-width, multiplexed buses of high and low volume logic devices

Chip-to-board (off-chip) speed (high-performance, peripheral buses)—Maximum signal I/O frequency to board peripheral buses of high and low volume logic devices

Other Attributes

Lithographic Field Size (mm^2)—Maximum single step or step-and-scan exposure area of a lithographic tool at the given technology node

Maximum Number Of Wiring Levels—On-chip interconnect levels including local interconnect, local and global routing, power and ground connections, and clock distribution

Fabrication Attributes And Methods

Electrical D_0 Defect Density (d/m^{-2})—Number of electrically significant defects per square meter at the given technology node, production life-cycle year, and target probe yield

Minimum Mask Count—Number of masking levels for mature production process flow with maximum wiring level (Logic)

Maximum Substrate Diameter (mm)

Bulk or Epitaxial or Silicon-on-Insulator Wafer—Silicon wafer diameter used in volume quantities by mainstream IC suppliers

Electrical Design And Test Metrics

Power Supply Voltage (V)

Minimum Logic V_{dd}— Nominal operating voltage of chips from power source for operation at design requirements

Maximum Power

High-performance with heat sink (W)—Maximum total power dissipated in high-performance chips with an external heat sink

Battery (W)—Maximum total power/chip dissipated in battery operated chips

Design And Test

Volume Tester Cost/Pin ($K/pin)—Cost of functional (chip sort) test in high volume applications divided by number of package pins.