Digital Electronics – Electronics, Devices and Circuits

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Introduction

- In the coming lectures we will consider how logic gates can be built using electronic circuits
- First, basic concepts concerning electrical circuits and components will be introduced
- This will enable the analysis of linear circuits, i.e., one where superposition applies:
  - If an input $x_1(t)$ gives an output $y_1(t)$, and input $x_2(t)$ gives an output $y_2(t)$, then input $[x_1(t)+x_2(t)]$ gives an output $[y_1(t)+y_2(t)]$

Introduction

- However, logic circuits are non-linear, consequently we will introduce a graphical technique for analysing such circuits
- Semiconductor materials, junction diodes and field effect transistors (FET) will be introduced
- The construction of an NMOS inverter from an n-channel (FET) will then be described
- Finally, CMOS logic built using FETs will then be presented

Basic Electricity

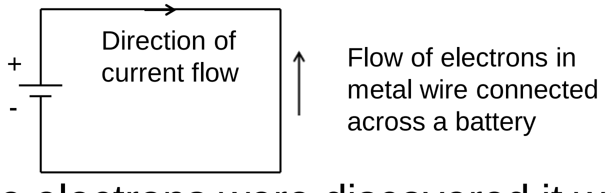
- An electric current is produced when charged particles (e.g., electrons in metals, or electrons and ions in a gas or liquid) move in a definite direction
- In metals, the outer electrons are held loosely by their atoms and are free to move around the fixed positive metal ions
- This free electron motion is random, and so there is no net flow of charge in any direction, i.e., no current flow

Basic Electricity

- If a metal wire is connected across the terminals of a battery, the battery acts as an 'electron pump' and forces the free electrons to drift toward the +ve terminal and in effect flow through the battery
- The drift speed of the free electrons is low, e.g., < 1 mm per second owing to frequent collisions with the metal ions.
- However, they all start drifting together as soon as the battery is applied

Basic Electricity

- The flow of electrons in one direction is known as an electric current and reveals itself by making the metal warmer and by deflecting a nearby magnetic compass



- Before electrons were discovered it was imagined that the flow of current was due to positively charged particles flowing out of +ve toward –ve battery terminal

Basic Electricity

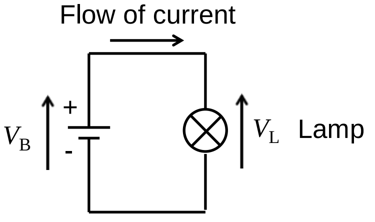
- Note that 'conventional' current flow is still defined as flowing from the +ve toward the –ve battery terminal (i.e., the opposite way to the flow of the electrons in the metal)!
- A huge number of charged particles (electrons in the case of metals) drift past each point in a circuit per second.
- The unit of charge is the *Coulomb* (C) and one electron has a charge of $1.6 * 10^{-19}$ C

Basic Electricity

- Thus one C of charge is equivalent to $6.25 * 10^{18}$ electrons
- When one C of charge passes a point in a circuit per second, this is defined as a current (I) of 1 *Ampere* (A), i.e., $I = Q/t$, where Q is the charge (C) and t is time in seconds (s), i.e., current is the rate of change of charge.

Basic Electricity

- In the circuit shown below, it is the battery that supplies the electrical force and energy that drives the electrons around the circuit.



- The electromotive force (emf) V_B of a battery is defined to be 1 *Volt* (V) if it gives 1 *Joule* (J) of electrical energy to each C of charge passing through it.

Basic Electricity

- The lamp in the previous circuit changes most of the electrical energy carried by the free electrons into heat and light
- The potential difference (pd) V_L across the lamp is defined to be 1 *Volt* (V) if it changes 1 *Joule* (J) of electrical energy into other forms of energy (e.g., heat and light) when 1 C of charge passes through it, i.e., $V_L=E/Q$, where E is the energy dissipated (J) and Q is the charge (C)

Basic Electricity

- Note that pd and emf are usually called *voltages* since both are measured in V
- The flow of electric charge in a circuit is analogous to the flow of water in a pipe. Thus a pressure difference is required to make water flow – To move electric charge we consider that a pd is needed, i.e., whenever there is a current flowing between 2 points in a circuit there must be a pd between them

Basic Electricity

- What is the power dissipated (P_L) in the lamp in the previous circuit?
- $P_L = E/t$ (J/s). Previously we have, $E = QV_L$, and so, $P_L = QV_L/t$ (W) .
- Now substitute $Q = It$ from before to give, $P_L = It\,V_L/t = IV_L$ (W) , an expression that hopefully is familiar

Basic Electricity

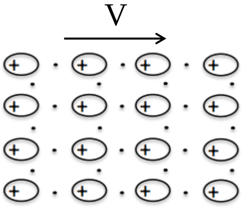
- So far, we have only considered metallic conductors where the charge is carried by ‘free’ electrons in the metal lattice.
- We will now consider the electrical properties of some other materials, specifically, *insulators* and *semiconductors*

Basic Materials

- The electrical properties of materials are central to understanding the operation of electronic devices
- Their functionality depends upon our ability to control properties such as their current-voltage characteristics
- Whether a material is a conductor or insulator depends upon how strongly bound the outer valence electrons are to their atomic cores

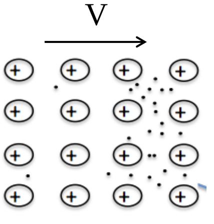
Insulators

- Consider a crystalline insulator, e.g., diamond
- Electrons are strongly bound and unable to move
- When a voltage difference is applied, the crystal will distort a bit, but no charge (i.e., electrons) will flow until breakdown occurs



Conductors

- Consider a metal conductor, e.g., copper
- Electrons are weakly bound and free to move
- When a voltage difference is applied, the crystal will distort a bit, but charge (i.e., electrons) will flow

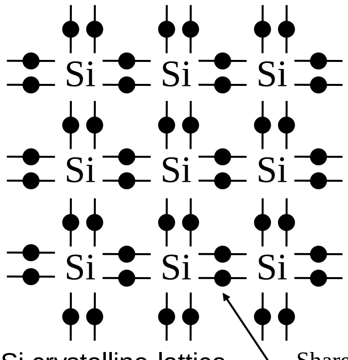


Semiconductors

- Since there are many free electrons in a metal, it is difficult to control its properties
- Consequently, what we need is a material with a low electron density, i.e., a semiconductor
- By carefully controlling the electron density we can create a whole range of electronic devices

Semiconductors

- Silicon (Si, Group IV) is a poor conductor of electricity, i.e., a *semiconductor*



Si crystalline lattice – poor conductor at low temperatures

Shared valence electron

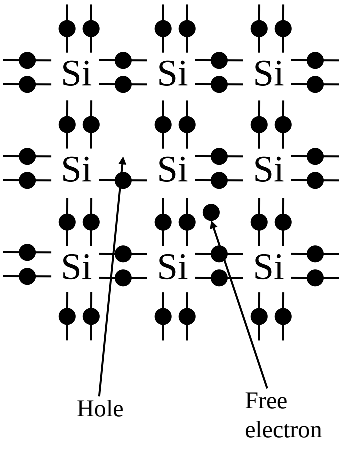
Si is *tetravalent*, i.e., it has 4 electrons in its *valance* band

Si crystals held together by *'covalent'* bonding

Recall that 8 valence electrons yield a stable state – each Si atom now appears to have 8 electrons, though in fact each atom only has a half share in them. Note this is a much more stable state than is the exclusive possession of 4 valence electrons

Semiconductors

- As temperature rises conductivity rises



As temperature rises, thermal vibration of the atoms causes bonds to break: electrons are free to wander around the crystal.

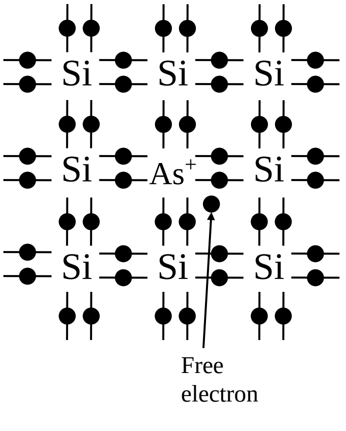
When an electron breaks free (i.e., moves into the *'conduction band'* it leaves behind a *'hole'* or absence of negative charge in the lattice

The hole can appear to move if it is filled by an electron from an adjacent atom

The availability of free electrons makes Si a conductor (a poor one)

n-type Si

- n-type silicon (Group IV) is doped with arsenic (Group V) that has an additional electron that is not involved in the bonds to the neighbouring Si atoms



The additional electron needs only a little energy to move into the conduction band.

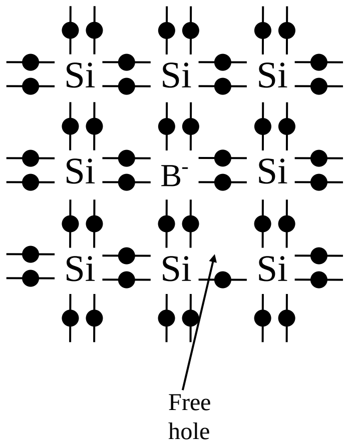
This electron is free to move around the lattice

Owing to its negative charge, the resulting semiconductor is known as *n-type*

Arsenic is known as a *donor* since it donates an electron

p-type Si

- p-type silicon (Group IV) is doped with boron (B, Group III)



The B atom has only 3 valence electrons, it accepts an extra electron from one of the adjacent Si atoms to complete its covalent bonds

This leaves a *hole* (i.e., absence of a valence electron) in the lattice

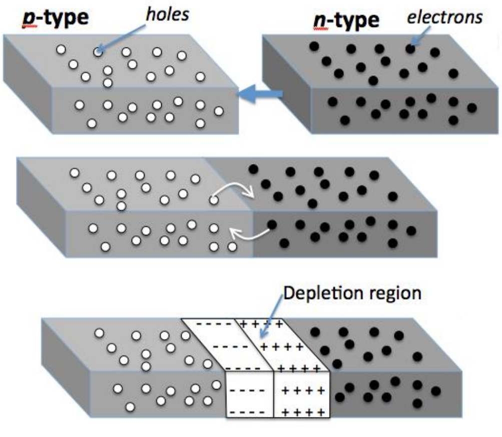
This hole is free to move in the lattice – actually it is the electrons that do the shifting, but the result is that the hole is shuffled from atom to atom.

The free hole has a positive charge, hence this semiconductor is *p-type*

B is known as an *acceptor*

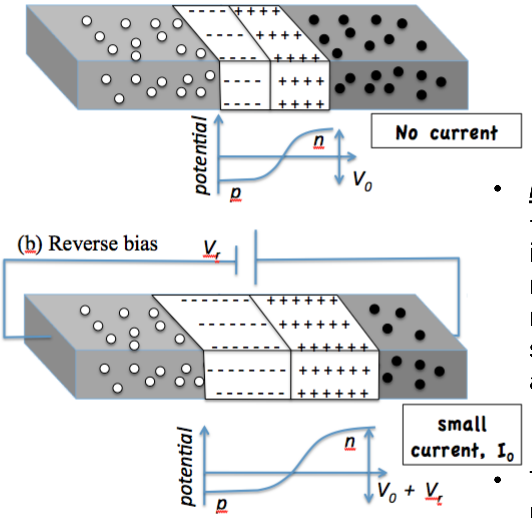
p-n Junction

- The key to building useful devices is combining p and n type semiconductors to form a p-n junction



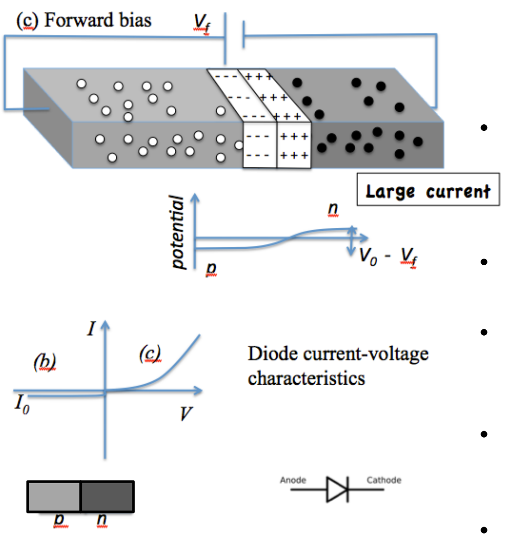
- Electrons and holes diffuse across junction due to large concentration gradient
- On n-side, diffusion out of electrons leaves +ve charged donor atoms
- On p-side, diffusion out of holes leaves -ve charged acceptor atoms
- Leaves a space-charge (depletion) region with no free charges
- Space charge gives rise to electric field that opposes diffusion
- Equilibrium is reached where no more charges move across junction
- The pd associated with field is known as 'contact potential'

Biased p-n Junction



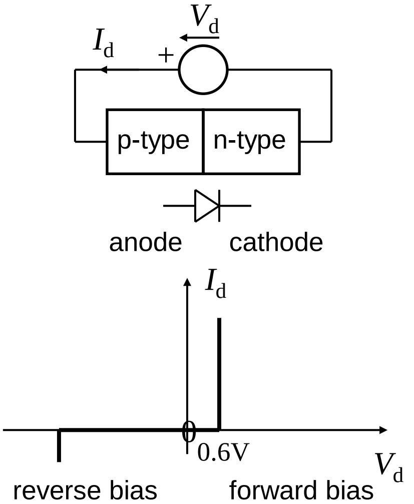
- ***Reverse bias***: By making n-type +ve, electrons are removed from it increasing size of space charge region. Similarly holes are removed from p-type region. Thus space charge region and its associated field are increased.
- The net current is known as the reverse saturation current – order of nA

Biased p-n Junction



- With ***forward bias***, on the p-side holes are pushed toward junction where they neutralise some of the –ve space charge.
- Similarly on the n-side, electrons are pushed toward the junction and neutralise some of the +ve space charge.
- So depletion region and associated field are reduced.
- This allows diffusion current to increase significantly and has the order of mA
- Thus the p-n junction allows significant current flow in only one direction
- This device is known as a ***diode***

Diode – Ideal Characteristic



Circuit Theory

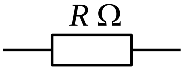
- Electrical engineers have an alternative (but essentially equivalent) view concerning pd.
- That is, conductors, to a greater or lesser extent, oppose the flow of current. This ‘opposition’ is quantified in terms of *resistance* (R). Thus the greater is the resistance, the larger is the potential difference measured across the conductor (for a given current).

Circuit Theory

- The *resistance* (R) of a conductor is defined as R=V/I, where V is the pd across the conductor and I is the current through the conductor.
- This is know as *Ohms Law* and is usually expressed as V=IR, where resistance is defined to be in Ohms (Ω).
- So for an *ohmic* (i.e., linear) conductor, plotting I against V yields a straight line through the origin

Circuit Theory

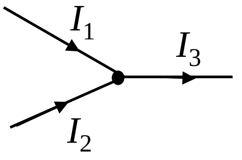
- Conductors made to have a specific value of resistance are known as *resistors*.
- They have the following symbol in an electrical circuit:



- Analogy:
  - The flow of electric charges can be compared with the flow of water in a pipe.
  - A pressure (voltage) difference is needed to make water (charges) flow in a pipe (conductor).

Circuit Theory

- Kirchhoff's Current Law – The sum of currents entering a junction (or node) is zero, e.g.,

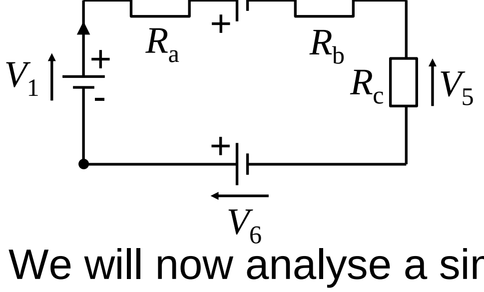


$I_1+I_2-I_3 = 0$ or $I_1+I_2 = I_3$

- That is, what goes into the junction is equal to what comes out of the junction – Think water pipe analogy again!

Circuit Theory

- Kirchhoff's Voltage Law – In any closed loop of an electric circuit the sum of all the voltages in that loop is zero, e.g.,

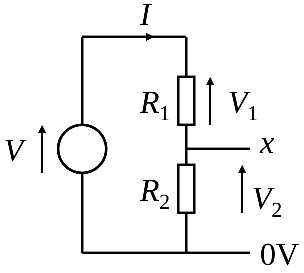


$V_1-V_2-V_3-V_4-V_5+V_6 = 0$

- We will now analyse a simple 2 resistor circuit known as a *potential divider*

Potential Divider

- What is the voltage at point x relative to the 0V point?



$$V = V_1 + V_2$$

$$V_1 = IR_1 \qquad V_2 = IR_2$$

$$V = IR_1 + IR_2 = I(R_1 + R_2)$$

$$I = \frac{V}{(R_1 + R_2)}$$

$$V_x = V_2 = \frac{V}{(R_1 + R_2)} R_2 = V\left(\frac{R_2}{R_1 + R_2}\right)$$

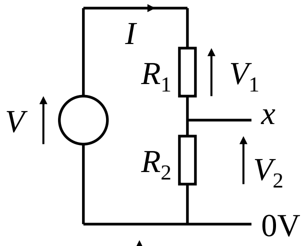
Note: circle represents an ideal voltage source, i.e., a perfect battery

Solving Non-linear circuits

- As mentioned previously, not all electronic devices have linear I-V characteristics, importantly in our case this includes the FETs used to build logic circuits
- Consequently we cannot easily use the algebraic approach applied previously to the potential divider. Instead, we will use a graphical approach
- Firstly though, we will apply the graphical approach to the potential divider example

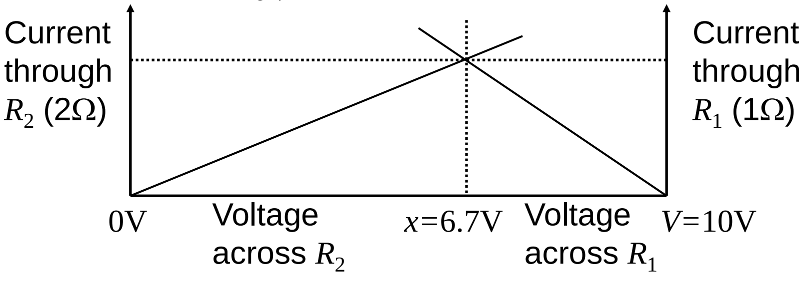
Potential Divider

- How can we do this graphically?



So if V = 10V, R_1 = 1Ω and R_2 = 2Ω

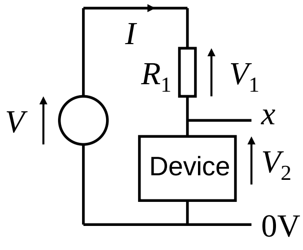
$$V_x = V\left(\frac{R_2}{R_1 + R_2}\right) = 10\left(\frac{2}{1+2}\right) = 6.7\text{V}$$



Graphical Approach

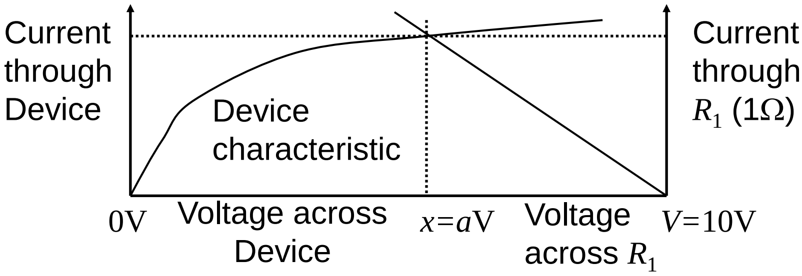
- Clearly approach works for a linear circuit.
- How could we apply this if we have a non-linear device, e.g., a transistor in place of R_2?
- What we do is substitute the V-I characteristic of the non-linear device in place of the linear characteristic (a straight line due to Ohm's Law) used previously for R_2

Graphical Approach



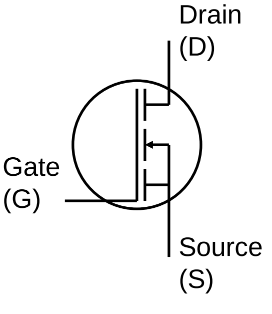
So if V = 10V and R_1 = 1Ω

The voltage at x is aV as shown in the graph



n-Channel MOSFET

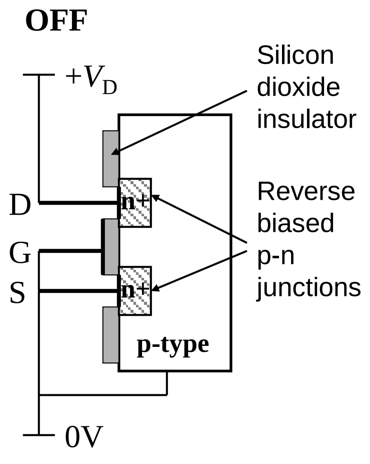
- We will now introduce a more complex semiconductor device known as an n-channel Metal Oxide Semiconductor Field Effect Transistor (MOSFET) and see how it can be used to build logic circuits



The current flow from D to S (I_{DS}) is controlled by the voltage applied between G and S (V_{GS})

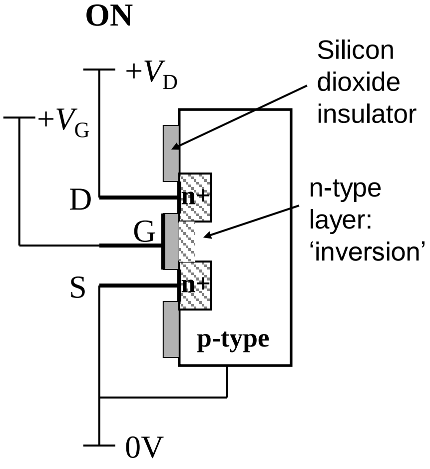
We will be describing enhancement mode devices in which no current flows (I_{DS}=0, i.e., the transistor is Off) when V_{GS}=0V

n-Channel MOSFET



Drain (and Source) diode reverse biased, so no path for current to flow from S to D, i.e., the transistor is **off**

n-Channel MOSFET



Consider the situation when the Gate (G) voltage (V_G) is raised to a positive voltage, say V_D

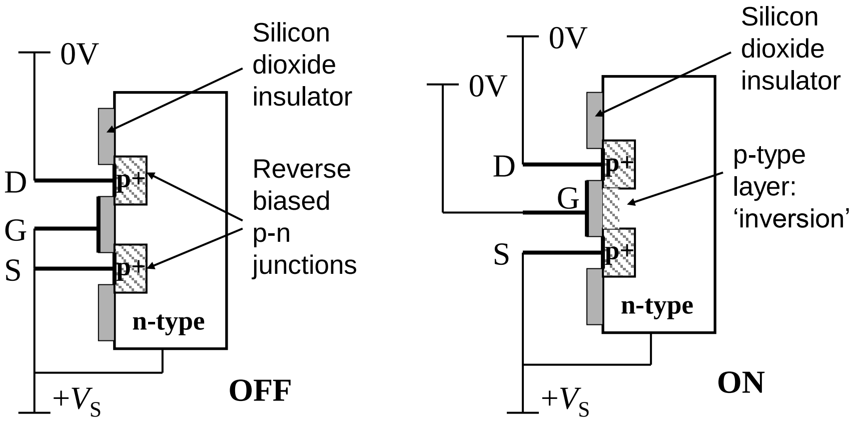
Electrons attracted to underside of the G, so this region is 'inverted' and becomes n-type. This region is known as the *channel*

There is now a continuous path from n-type S to n-type D, so electrons can flow from S to D, i.e., the transistor is **on**

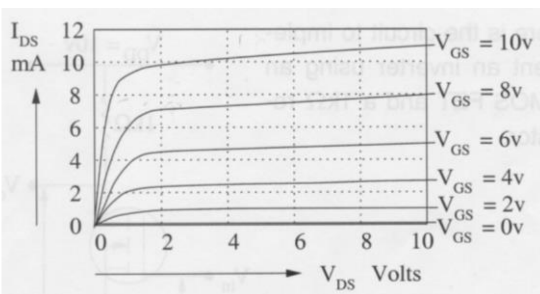
The G voltage (V_G) needed for this to occur is known as the *threshold voltage* (V_t). Typically 0.3 to 0.7 V.

p-Channel MOSFET

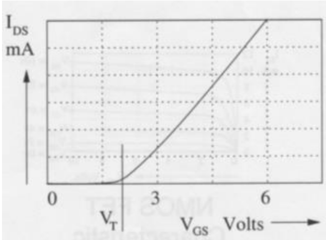
- Two varieties, namely p and n channel
- p-channel have the opposite construction, i.e., n-type substrate and p-type S and D regions



n-MOSFET Characteristics



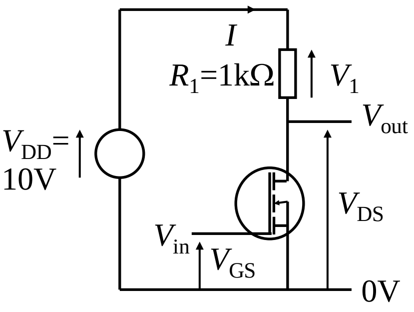
Plots V-I characteristics of the device for various Gate voltages (V_{GS})

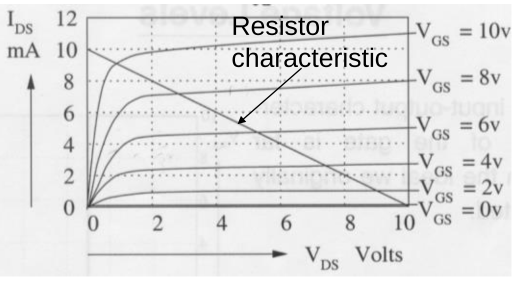


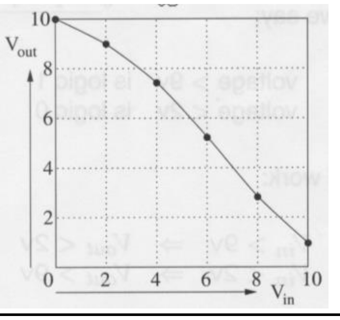
At a constant value of V_{DS} , we can also see that I_{DS} is a function of the Gate voltage, V_{GS}

The transistor begins to conduct when the Gate voltage, V_{GS} , reaches the Threshold voltage: V_T

n-MOS Inverter







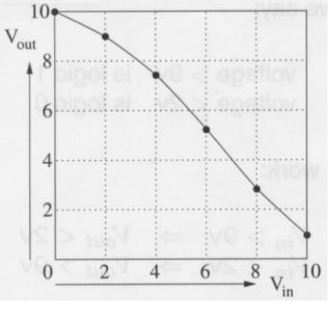
Note V_{in}=V_{GS} and V_{out}=V_{DS}

We can use the graphical approach to determine the relationship between V_{in} and V_{out}

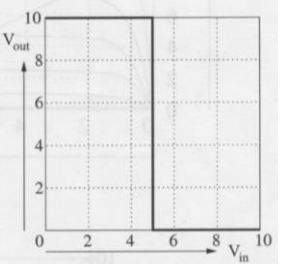
n-MOS Inverter

- Note it does not have the ‘ideal’ characteristic that we would like from an ‘inverter’ function

Actual



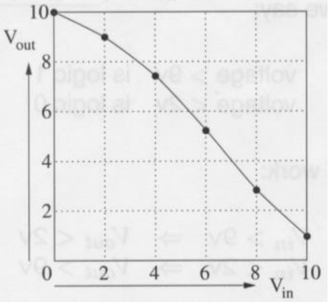
Ideal



However if we specify suitable voltage thresholds, we can achieve a ‘binary’ action.

n-MOS Inverter

Actual



So if we say:

voltage > 9V is logic 1

voltage < 2V is logic 0

The gate will work as follows:

V_{in} > 9V then V_{out} < 2V and if

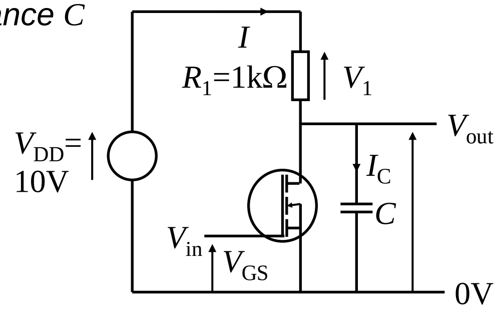
V_{in} < 2V then V_{out} > 9V

n-MOS Logic

- It is possible (and was done in the early days) to build other logic functions, e.g., NOR and NAND using n-MOS transistors
- However, n-MOS logic has fundamental problems:
  - Speed of operation
  - Power consumption

n-MOS Logic

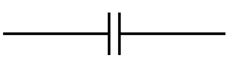
- One of the main speed limitations is due to stray capacitance owing to the metal track used to connect gate inputs and outputs. This has a finite capacitance to ground, i.e., the 0V connection.
  - We modify the circuit model to include this *stray capacitance C*



- To see the effect of stray capacitance, we first consider the electrical properties of capacitors.

Devices that store energy

- Some common circuit components store energy, e.g., capacitors and inductors.
- We will now consider capacitors in detail.
- The physical construction of a capacitor is effectively 2 conductors separated by a non-conductor (or dielectric as it is known).



Symbol of a Capacitor

Unit of capacitance: Farads (F)

- Electrical charge can be stored in such a device.

Capacitors

- So, parallel conductors brought sufficiently close (but not touching) will form a capacitor
- Parallel conductors often occur on circuit boards (and on integrated circuits), thus creating unwanted (or parasitic) capacitors.
- We will see that parasitic capacitors can have a significant negative impact on the switching characteristics of digital logic circuits.

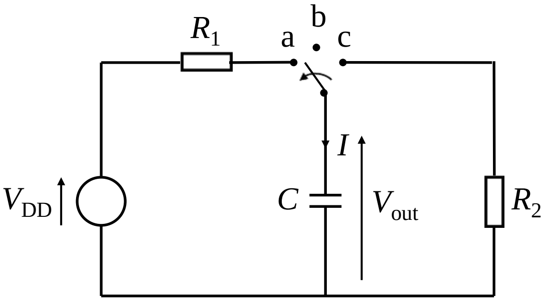
Capacitors

- The relationship between the charge Q stored in a capacitor C and the voltage V across its terminals is $Q = VC$.
- As mentioned previously, current is the rate of flow of charge, i.e., $\mathrm{d}Q/\mathrm{d}t = I$, or alternatively, $Q = \int I dt$.
- So we can write,

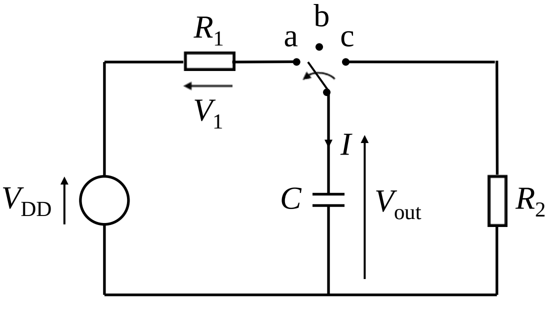
$$V = \frac{1}{C}\int I dt$$

Capacitors

- We now wish to investigate what happens when sudden changes in configuration occur in a simple resistor-capacitor (RC) circuit.

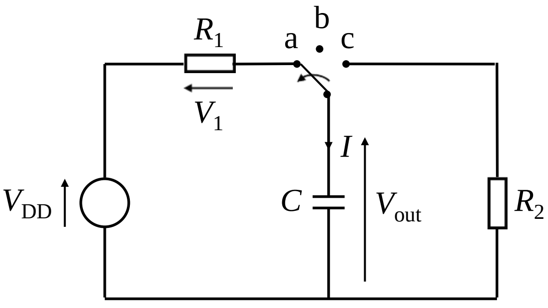


RC circuits



- Initially, C is discharged, i.e., V_{out}=0 and the switch moves from position b to position a
- C charges through R_1 and current I flows in R_1 and C

RC circuits



$$V_{DD} - V_1 - V_{out} = 0$$

$$V_{DD} = V_1 + V_{out}$$

Sub for V_{out} in terms of I and C (from earlier eqn.)

$$V_{DD} = IR_1 + \frac{1}{C}\int I dt$$

Differentiate wrt t gives

$$0 = R_1 \frac{dI}{dt} + \frac{I}{C}$$

Then rearranging gives

$$-\frac{dt}{CR_1} = \frac{dI}{I}$$

RC circuits

Integrating both sides of the previous equation gives

$$-\frac{t}{CR_1} + a = \ln I$$

We now need to find the integration constant a .

To do this we look at the initial conditions at $t = 0$, i.e., V_{out}=0. This gives an initial current I_0=V_{DD}/R_1

$$a = \ln I_0 = \ln\left(\frac{V_{DD}}{R_1}\right)$$

So,

$$-\frac{t}{CR_1} + \ln I_0 = \ln I$$

$$-\frac{t}{CR_1} = \ln \frac{I}{I_0}$$

Antilog both sides,

$$e^{-t/CR_1} = \frac{I}{I_0}$$

$$I = I_0 e^{-t/CR_1}$$

RC circuits

Now,

$$V_{out} = V_{DD} - V_1$$

and,

$$V_1 = IR_1$$

Substituting for V_1 gives,

$$V_{out} = V_{DD} - IR_1$$

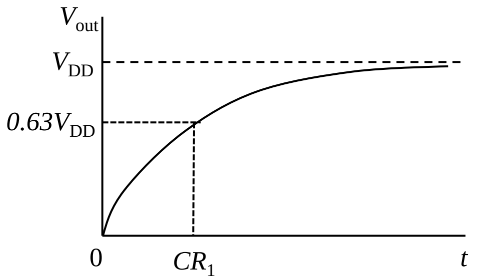
$$V_{out} = V_{DD} - R_1 I_0 e^{-t/CR_1}$$

Substituting for I_0 gives,

$$V_{out} = V_{DD} - R_1 \frac{V_{DD}}{R_1} e^{-t/CR_1}$$

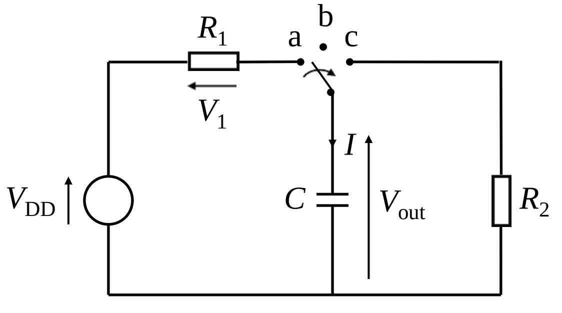
$$V_{out} = V_{DD}\left(1 - e^{-t/CR_1}\right)$$

Plotting yields,



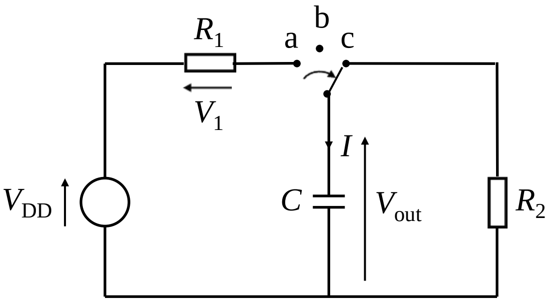
CR_1 is knows as the time constant – has units of seconds

RC circuits

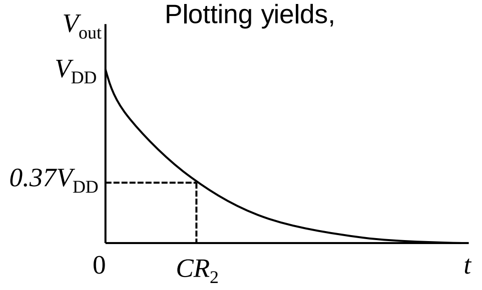


- Initially assume C is fully charged, i.e., $V_{out}=V_{DD}$ and the switch moves from position a to position c
- C discharges through R_2 and current flows in R_2 and C

RC circuits



Plotting yields,



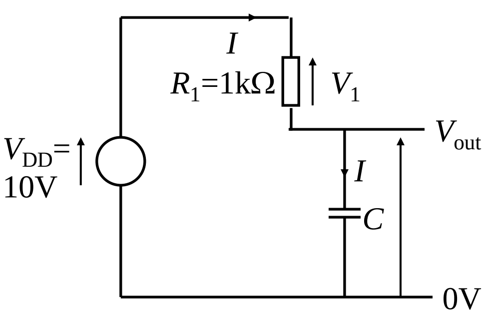
The expression for V_{out} is,

$$V_{out} = V_{DD} e^{-t/CR_2}$$

n-MOS Logic

- To see the effect of this stray capacitance we will consider what happens when the transistor is ON (so that V_{out}=0V at beginning), then turned OFF and then turned ON again
- When the transistor is OFF it is effectively an open circuit, i.e., we can eliminate if from the circuit diagram

Transistor turned OFF



The problem with capacitors is that the voltage across them cannot change instantaneously.

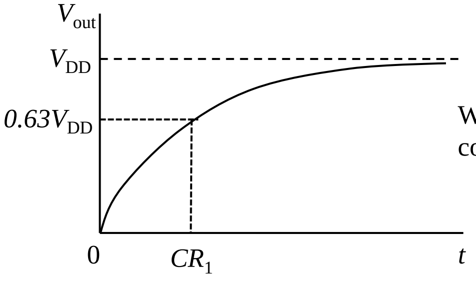
The ‘stray’ capacitor C charges through R_1. Note C is initially discharged, i.e., V_{out}=0V

n-MOS Logic

- Using the previous result for a capacitor charging via a resistor we can write:

$$V_{out} = V_{DD}\left(1 - e^{-t/CR_1}\right)$$

Plotting yields,

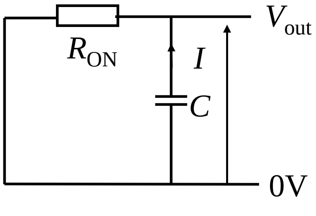


Where CR_1 is known as the time constant – has units of seconds

n-MOS Logic

- When the transistor is ON it is effectively a low value resistor, R_{ON}. (say < 100Ω)
- We will assume capacitor is charged to a voltage V_{DD} just before the transistor is turned ON

Transistor turned ON again

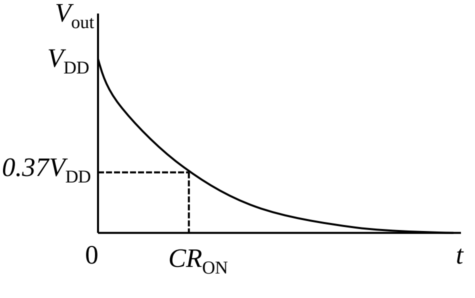


'Stray' capacitor C discharges through R_{ON}

The expression for V_{out} is,

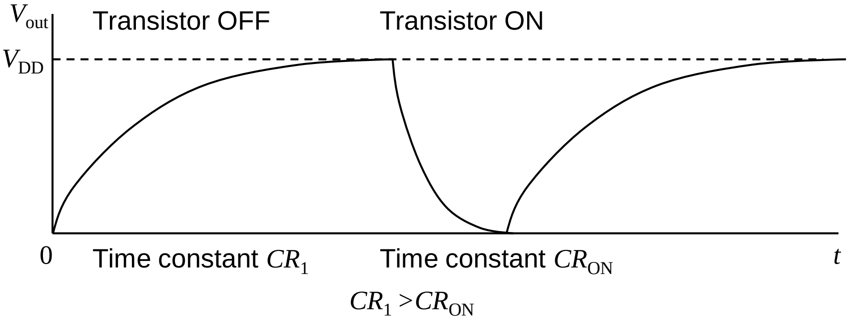
$$V_{out} = V_{DD}e^{-t/CR_{ON}}$$

Plotting yields,



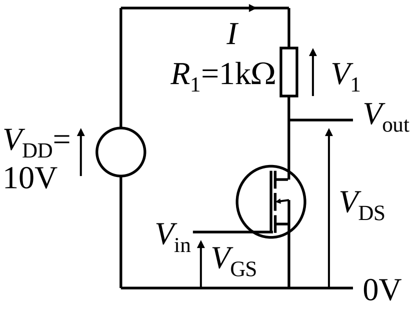
n-MOS Logic

- When the transistor turns OFF, C charges through R_1. This means the rising edge is slow since it is defined by the large time constant R_1C (since R_1 is high).
- When the transistor turns ON, C discharges through it, i.e., effectively resistance R_{ON}. The speed of the falling edge is faster since the transistor ON resistance (R_{ON}) is low.



n-MOS Logic

- Power consumption is also a problem



Transistor OFF

No problem since no current is flowing through R_1, i.e., V_{out} = 10V

Transistor ON

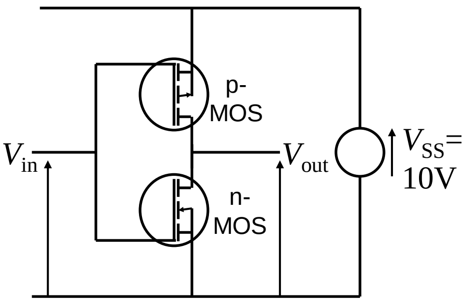
This is a problem since current is flowing through R_1 . For example, if V_{out} = 1V (corresponds with V_{in} = 10V and $I_D = I$ = 9mA), the power dissipated in the resistor is the product of voltage across it and the current through it, i.e.,

$$P_{disp} = I \times V_1 = 9 \times 10^{-3} \times 9 = 81\,\mathrm{mW}$$

CMOS Logic

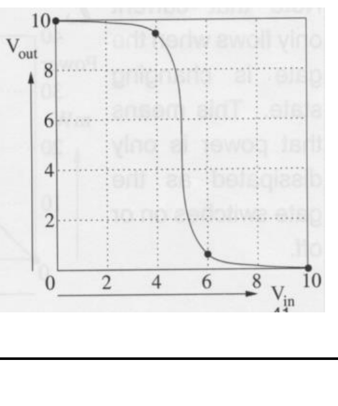
- To overcome these problems, complementary MOS (CMOS) logic was developed
- As the name implies it uses p-channel as well as n-channel MOS transistors
- Essentially, p-MOS transistors are n-MOS transistors but with all the polarities reversed!

CMOS Inverter



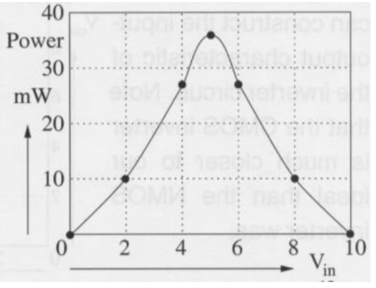
V_{in}	N-MOS	P-MOS	V_{out}
low	off	on	high
high	on	off	low

Using the graphical approach we can show that the switching characteristics are now much better than for the n-MOS inverter



CMOS Inverter

- It can be shown that the transistors only dissipate power while they are switching.



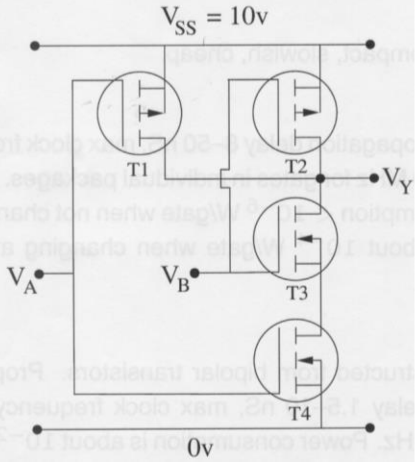
This is when both transistors are on. When one or the other is off, the power dissipation is zero

CMOS is also better at driving capacitive loads since it has active transistors on both rising and falling edges

CMOS Gates

- CMOS can also be used to build NAND and NOR gates
- They have similar electrical properties to the CMOS inverter

CMOS NAND Gate



V_A	V_B	T1	T2	T3	T4	V_Y
low	low	on	on	off	off	high
low	high	on	off	on	off	high
high	low	off	on	off	on	high
high	high	off	off	on	on	low

Logic Families

- **NMOS** – compact, slow, cheap, obsolete
- **CMOS** – Older families slow (4000 series about 60ns), but new ones (74AC) much faster (3ns). 74HC series popular
- **TTL** – Uses bipolar transistors. Known as 74 series. Note that most 74 series devices are now available in CMOS. Older versions slow (LS about 16ns), newer ones faster (AS about 2ns)
- **ECL** – High speed, but high power consumption

Logic Families

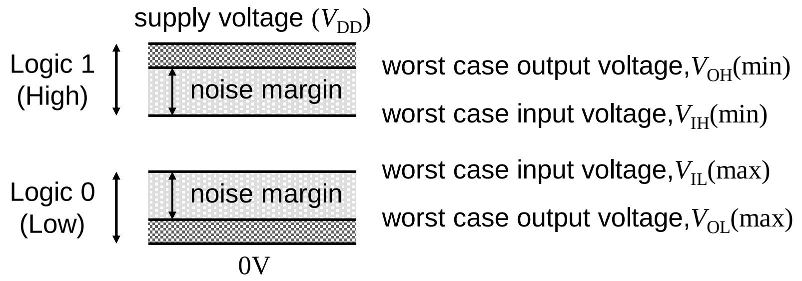
- Best to stick with the particular family which has the best performance, power consumption cost trade-off for the required purpose
- It is possible to mix logic families and sub-families, but care is required regarding the acceptable logic voltage levels and gate current handling capabilities

Meaning of Voltage Levels

- As we have seen, the relationship between the input voltage to a gate and the output voltage depends upon the particular implementation technology
- Essentially, the signals between outputs and inputs are ‘analogue’ and so are susceptible to corruption by additive noise, e.g., due to cross talk from signals in adjacent wires
- What we need is a method for quantifying the tolerance of a particular logic to noise

Noise Margin

- Tolerance to noise is quantified in terms of the noise margin



Logic 0 noise margin = V_{IL}(max) - V_{OL}(max)

Logic 1 noise margin = V_{OH}(min) - V_{IH}(min)

Noise Margin

- For the 74 series High Speed CMOS (HCMOS) used in the hardware labs (using the values from the data sheet):

Logic 0 noise margin = V_{IL}(max) - V_{OL}(max)

Logic 0 noise margin = 1.35 – 0.1 = 1.25 V

Logic 1 noise margin = V_{OH}(min) - V_{IH}(min)

Logic 1 noise margin = 4.4 – 3.15 = 1.25 V

See the worst case noise margin = 1.25V, which is much greater than the 0.4 V typical of TTL series devices. Consequently HCMOS devices can tolerate more noise pick-up before performance becomes compromised

Interfacing to the 'Analogue World'

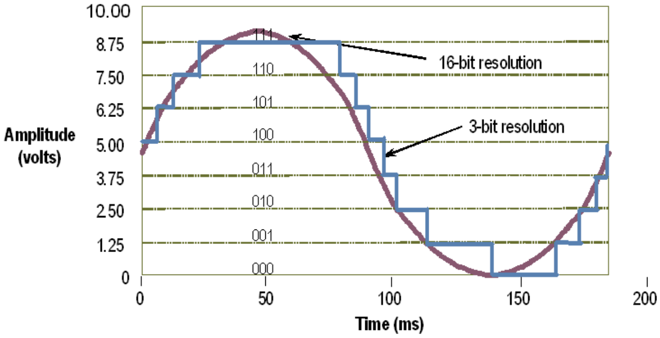
- Digital electronic systems often need to interface to the 'analogue' real world. For example:
  - To convert an analogue audio signal to a digital format we need an analogue to digital converter (ADC)
  - Similarly to convert a digitally represented signal into an analogue signal we need to use a digital to analogue converter (DAC)
- ADCs and DACs are implemented in various ways depending upon factors such as conversion speed, resolution and power consumption

Analogue to Digital Conversion

- ADC is a 2 stage process:
  - Regular sampling to convert the continuous time analogue signal into a signal that is discrete in time, i.e., it only exists at multiples of the sample time T. Thus x(t) can be represented as x(0), x(T), x(2T), x(3T)….
  - These sample values can still take continuous amplitude values, hence the next step is to represent them using only discrete values in the amplitude domain. To do this the samples are quantised in amplitude, i.e., they are constrained to take one of only M possible amplitude values
  - Each of these discrete amplitude levels is represented by an n-bit binary code
  - Thus in an n-bit ADC, there are $M=2^n$ quantisation levels

Analogue to Digital Conversion

- Thus the ADC process introduces 'quantisation error' owing to the finite number of possible amplitude levels that can be represented
- The greater is the number of quantisation levels (i.e., 'bits' in the ADC), the lower will be the quantisation error, but at the cost of a higher bit rate



Analogue to Digital Conversion

- In addition, the sample rate (1/T) must be at least twice the highest frequency in the analogue signal being sampled – known as the Nyquist rate
- To ensure this happens, the analogue signal is often passed through a low pass filter that will remove frequencies above a specified maximum
- If the Nyquist rate is not satisfied, the sampled signal will be subject to 'alias distortion' that cannot be removed and will be present in the reconstructed analogue signal

Analogue to Digital Conversion

- The ADC also requires that the input signal suits its specified amplitude range. Usually, the ADC has a range covering several Volts, while the signal from the transducer can be of the order of mV
- Consequently, amplification (a voltage gain>1) of the analogue signal is usually required before being input to the ADC
- If not, the digitised signal will have poor quality (i.e., a low signal to quantisation noise ratio)
- Operational amplifier based ‘Gain blocks’ in front of the ADC are often used since they have predictable performance and are straightforward to use

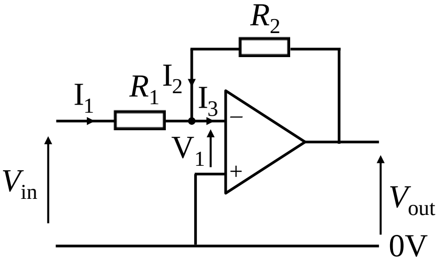
Digital to Analogue Conversion

- A DAC is used to convert the digitised sample values back to an analogue signal.
- A low pass filter (one that removes high frequencies) usually follows the DAC to yield a smooth continuous time signal
- Operational amplifier based buffer amplifiers are also often used following the DAC to prevent the load (e.g., transducers such as headphones) affecting the operation of the DAC

Operational Amplifier Circuits

- Operational amplifiers (or 'Op-Amps) have 2 inputs (known as inverting (-) and non-inverting (+)) and a single output
- They can be configured to implement gain blocks (i.e., amplifiers) and many other functions, e.g., filters, summing blocks
- We will now look at several common op-amp based amplifier configurations, specifically inverting, non-inverting and unity gain buffer
- We will assume the use of 'ideal' op-amps, i.e., infinite input resistance (zero input current) and infinite gain.

Inverting Amplifier



$I_1 + I_2 - I_3 = 0$

Now, $I_3 = 0$ since the input resistance of the op amp is ∞, so

$I_1 = -I_2$

$V_{in} - I_1 R_1 - V_1 = 0$ and

$V_1 + I_2 R_2 - V_{out} = 0$

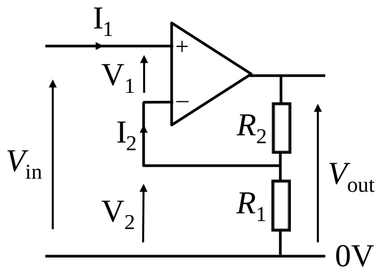
Now, $V_1 = 0$ since the op-amp has ∞ gain (virtual earth assumption)

$V_{in} = I_1 R_1$ and $V_{out} = I_2 R_2 = -I_1 R_2$

So, $I_1 = -\frac{V_{out}}{R_2}$

Yielding, $V_{in} = -\frac{V_{out} R_1}{R_2}$ Voltage gain, $\frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1}$

Non-Inverting Amplifier



Now, $I_1 = I_2 = 0$ since the input resistance of the op amp is ∞, so

$$V_2 = V_{out}\frac{R_1}{R_1 + R_2}$$

$$V_{in} - V_1 - V_2 = 0$$

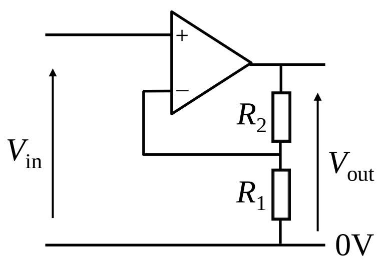
Now, $V_1 = 0$ since the op-amp has ∞ gain (virtual earth assumption)

$V_2 = V_{in}$

So, $V_{in} = V_{out}\dfrac{R_1}{R_1 + R_2}$

Yielding, $\dfrac{V_{out}}{V_{in}} = \dfrac{R_1 + R_2}{R_1}$ Voltage gain, $\dfrac{V_{out}}{V_{in}} = 1 + \dfrac{R_2}{R_1}$

Buffer Amplifier (Unity Gain)

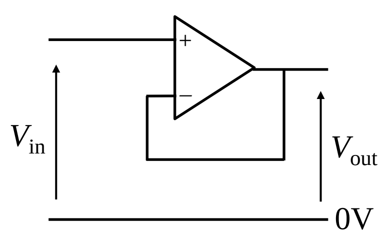


We know the voltage gain for the non-inverting amplifier is,

$$\frac{V_{out}}{V_{in}} = 1 + \frac{R_2}{R_1}$$

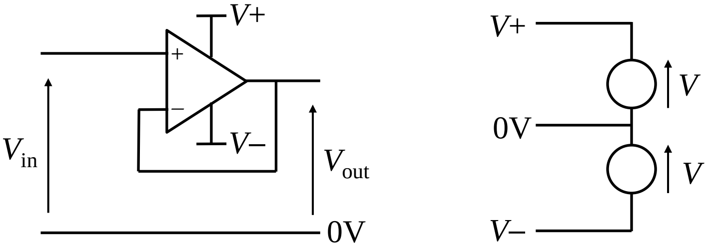
Now, if we let $R_2 = 0$ (a short circuit) and $R_1 = \infty$ (open circuit) then

$$\frac{V_{out}}{V_{in}} = 1$$



Op-Amp Power Supplies

- Usually, op-amps use split power supplies, i.e., +ve and –ve power supply connections



- This permits input signals having both +ve and –ve excursions to be amplified
- This can be inconvenient for battery powered equipment. However, if the input signal is for e.g., always +ve, the V– rail can removed i.e., set to 0V

Op-Amp Applications

- As mentioned, op-amps can be used in many other common analogue signal processing tasks, for example:
  - Filters: circuits that can manipulate the frequency content of signals
  - Mathematical functions, e.g., integrators and differentiators
  - Comparators and triggers, i.e., thresholding devices
- A 'cookbook' of useful such applications can be found in 'The Art of Electronics' by Horowitz and Hill