ESL and TLM Exercises - Quick Questions

ESLq1. Briefly explain how and why an ESL model that uses a TLM model of its busses can run the embedded software with no modification to its device drivers.

ESLq2. What, if any, do the following RTL concepts play in ESL modelling? a) 4-valued logic, b) cycle-accurate model, c) structural netlist.

ESLq3. Explain how the device driver for an on-chip network might be modified if the network device itself is not to be modelled and instead transactions are to be used to directly pass packets between network nodes. [In the lectures notes, for a single endpoint, this was described as a mid-level model, but here we go further and do not model the network.] What sort of model is logically above and below a mid-level model?

ESLq4. Show how a user-defined, abstract datatype can be passed along a SystemC channel by sketching several lines of code for a packet switch, router or demultiplexer. *This was not lectured and is not examinable this year.*

ESLq5. What problems might arise when using high-level models of systems that use dynamic code loading and self-modifying code?

ESLq6. What is the purpose and effect of the timing quantum in the loosely-timed model? Why might a transactional system exhibit different behaviour as the quantum is adjusted? Is this useful or just bad?

ESLq7. How would a static RAM TLM model behave differently when the modelled supply voltate is 0.9 compared with 1.2 volts?

ESLq8. What minimal parts of a system need to be modelled to get very accurate cache-hit metrics?

ESLq9. Why do we wish to get power figures without a SAIF file?

High-Level Synthesis Exercises - Quick Questions

HLSq1. What is binding step during HLS? What suffers if it is done poorly?

HLSq2. Why do HLS tools seek parallelism?

HLSq3. When can a structural resource be freely replicated by the HLS tool?

HLSq4. General C code is known to suffer from alias problems. What does this mean and why might it degrade HLS?

HLSq5. Why has HLS traditionally been restricted to manifestly finite-state subsystems?

HLSq6. Will a classical datapath and sequencer approach generate fully-pipelined solutions?

HLSq7. Why does an HLS solution typically consume at least an order of magnitude less power than a software implementation?

HLSq8. Why does an HLS solution sometimes provided much greater parallelism and/or performance than a software solution?

HLSq9. Why has Amazon just launched an FPGA-in-the-cloud service (EC2 F1)?

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