SoC D/M Exercise Sheet, 2014/2015

This sheet contains exercises of various lengths. Many exercises are nominally allocated marks at Tripos examination level (i.e. with 20 marks making a full exam question).

There is some repetition of material between the exercises, so a suitable target is to solve approximately one third of them. Exercises marked with a ♡ form a recommended core. Some sections contain additional preference instructions.

Example answers are available to supervisors.

SP3: Silicon Energy, Power and Technology

Power Estimation and Control questions:

POWER.1. Dynamic Clock Gating.

a) What is dynamic clock gating and why is it used ? [4 Marks]

b) Compare coarse-grained manual and fine-grained automatic clock gating. [4 Marks]

c) Describe some common clock-gate insertion transformations. [6 Marks]

d) Compare dynamic clock gating with power isolation islands in terms of automation, scale and functionality. [6 Marks]

POWER.2. ♡ : VLSI Energy Use. For this question, use the following figures and assume values for or look up values of any other information that you feel you need. Credit is awarded for the method and not for the numerical results.

Parameter	Value	Unit
Drawn Gate Length	0.08	μm
Metal Layers	6 to 9	layers
Gate Density	400K	gates/mm^2
Track Width	0.25	μm
Track Spacing	0.25	μm
Gate Output Capacitance	0.06	fF
Gate Input Capacitance	0.03	fF
Tracking Capacitance	1	fF/mm
Core Supply Voltage	0.9 to 1.4	V
FO4 Delay	51	ps
Leakage current	21	nA/gate

A processor core in the above technology uses 200k gates, excluding cache memories. It has two operating conditions: 100 MHz at 0.9 volts or 400 MHz at 1.4 volts. The average net activity ratio during halt is negligible and 0.3 when running.

Give all working and intermediate results. State any additional assumptions you need or use.

a) Estimate the area of the processor. [2 Marks]

b) Compute the power consumed per gate at each operating condition when driving a tracks of 0 mm and 1 mm. [2 Marks]

c) Estimate the power consumption of the processor core when halted and running for each operating condition. [3 Marks]

d) Compared with having the processor running at full performance all the time, how much power is saved just by halting the processor when it is idle ? [2 Marks]

e) How much power is saved by dynamic frequency scaling ? [2 Marks]

f) How does dynamic frequency scaling compare with halting ? [2 Marks]

g) How much power is saved by combined dynamic voltage and frequency scaling ? [2 Marks]

h) How much power might be saved by power gating (i.e. power isolation) ? [2 Marks]

i) Estimate the relative costs of performing a 32 bit addition and sending the 32 bit result 1 mm over the chip [3 Marks]

POWER.3. : Dynamic Voltage and Frequency Scaling.

a) Give a formula for the power dissipation associated with a net on a silicon chip. [3 Marks]

b) What is meant by dynamic clock gating and compare this to a technique where software writes to a control register to turn off a clock generator ? [3 Marks]

c) For a fixed supply voltage, quantify the power benefits of frequency scaling. In other words, compare computing quickly and halting with computing more-slowly and finishing just in time. [3 Marks]

d) Give two ways that the supply voltage to a region may be varied? [3 Marks]

e) Using variable supply voltages, quantify the power benefits of frequency scaling. [3 Marks]

f) In supervisions, discuss the architecture of an ASIC (or part of) that uses all of these techniques. [5 Marks]

POWER.4. : Power Consumption

This question is primarily for discussion in supervisions.

a) What are the main components of power consumption in a laptop computer? [5 Marks]

b) How does clock frequency affect power consumption ? [5 Marks]

c) How might clock frequency be controller in a laptop and for what reasons ? [5 Marks]

d) When viewing a DVD (including moving video and audio) on a laptop, what is the best clock frequency policy? [5 Marks]

POWER.5. Technology/Scaling.

This question is primarily for discussion in supervisions.

a) What is meant by the term *feature size* in VLSI ? Give typical values. [5 Marks]

b) What are the main consequences of moving to a smaller feature size in VLSI fabrication ? [5 Marks]

c) What happens to the relative costs of computation and communication as features get smaller ? [5 Marks]

d) Why has parallel computation become more important than ever before ? [5 Marks]

POWER.6. ♡ Battery Life Planning

a) Data can be compressed before being sent by a hand-held unit over a radio link or later on at a central server. What are the advantages and disadvantages? [4 Marks]

b) How might you estimate the battery life of a sensor device that has a 3 Watt radio transmitter, no LEDs or displays and needs to run about five minutes worth of CPU cycles per day? Would solar cells serve it well? [4 Marks]

c) In the last decade or so, digital sensors with radio (wireless) backlinks have been installed in all rooms in all public buildings. What have been the main forward steps in technology that have faciliated this? Does the price of copper make a difference? [3 Marks]

 END OF DOCUMENT.