SoC D/M Exercise Sheet, 2014/2015

This sheet contains exercises of various lengths. Many exercises are nominally allocated marks at Tripos examination level (i.e. with 20 marks making a full exam question).

There is some repetition of material between the exercises, so a suitable target is to solve approximately one third of them. Exercises marked with a ♡ form a recommended core. Some sections contain additional preference instructions.

Example answers are available to supervisors.

SP2: SoC Busses, Partition and Technology

Slide Pack SP2: This sheet should be tackled for the second supervision. Supervisors are recommended to set just the few exercises marked with ♡ with the remainder of the questions being available for brief discussion or self-study revision purposes.

This year SystemC is being lectured at the end, so please leave the SystemC parts of this sheet for now and answer again after that has been lectured.

SOC-SP2.1. ♡ : SoC Structure.

a) Sketch the block diagram for a SoC with one processor, one SRAM, one ROM, one Counter/Timer block and one PIO section, all connected to a single bus without any bus bridges. [5 Marks]

b) List the (main) net-level interface signals needed for a bus port that enables multiple bus operations to be in flight at once (such as the BVCI port lectured, or an IP block interface of similar functionality) and explain the protocol. [6 Marks]

c) Is it appropriate for DMA to be supported or used in the SoC of part *a)* ? [3 Marks]

d) How are interrupt signals routed in the SoC of part *a)* ? [3 Marks]

e) What modifications are needed if a second processor core were to be added ? Is a second bus a good idea ? [3 Marks]

SOC-SP2.2. : Multiple Busses With Bridges.

a) In SoC terms, what is a bus and how does it compare with the 1980's concept of a motherboard bus (such as the ISA or PCI bus) ? [2 Marks]

b) How might the destination port for a transaction over such a bus be decided ? [2 Marks]

c) What is a bus bridge, what transactions might it support and what internal operations might it implement ? [4 Marks]

d) If a SoC is designed with a number of bridged busses, what are the main aspects that determine the allocation of initiators and targets to the busses ? [3 Marks]

e) Is there no real difference between a Network On Chip and a set of bus bridges ? [3 Marks]

f) What form of bus protocol is needed for good performance on a SoC that uses a number of bridges busses or clock domains ? [3 Marks]

g) How is contention for destinations handled in a SoC that uses a number of bridges busses compared with a NoC (network on chip) ? [3 Marks]

SOC-SP2.3. : Network-On-Chip (NoC).

a) What is meant by the term Network-on-Chip and what are the main differences between using a number of bus bridges and a network fabric? [5 Marks]

b) Describe two buffering techniques that might be used in a NoC ? [2 Marks]

c) Describe a flow control technique used in a NoC ? [2 Marks]

SOC-SP2.4. : DRAM and Cache.

a) What are the main features of DRAM and why was it not commonly integrated as part of a SoC ? [5 Marks]

b) Why should out-of-order read responses ideally be supported by a SoC Bus or NoC ? [5 Marks]

c) Using a system clock of 400 MHz, a 32 bit MIPS/ARM-like CPU is served without a cache by a 16-bit DRAM system with the following parameters

Operation	Clock cycles	Function
RAS	3	Sending row address,
CAS	1	Read or write 16 bits in current row,
RAS precharge	2	Write back time when finished with row.

Making some assumptions about the pattern of access that the processor will make of the memory, estimate its performance in terms of instructions per second. [5 Marks]

d) If all instructions for inner loops are copied to a 32-bit wide on-chip SRAM (that provides true random access at 400 MHz) at code start, what is the performance now. [5 Marks]

e) If a cache structure with 98 percent instruction and 80 percent data hit rate is applied, what processor performance is now achieved ? You may consider in-order and out-of-order processors but full credit awarded for either. [5 Marks]

SOC-SP2.5. : JTAG Port and Test Modes. *(In lectures JTAG was only briefly mentioned in relationship to debugging and GDB remote serial protocol (RSP)). This question is suitable for discussion in supervisions but the material was not lectured.*

a) Why do ASICs commonly support special test modes? [4 Marks]

b) Define and compare boundary scan with full scan test path [4 Marks]

c) Briefly describe the structure and operation of the JTAG test port used on many chips. [4 Marks]

d) How can JTAG ports be combined and is this a good idea within a single SoC ? [4 Marks]

e) What other uses can the JTAG port frequently be put to ? [4 Marks]

SOC-SP2.6. : Cell Library.

a) Give a short list of logic cells to be found in a standard cell library. [5 Marks]

b) List five types of information that should be stored about each cell. [5 Marks]

c) Name several illustrative, specialist VLSI structures or components that cannot readily be made out of standard logic cells and explain why custom design is needed. [5 Marks]

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