L41: Lab 3 - Microarchitectural implications of IPC

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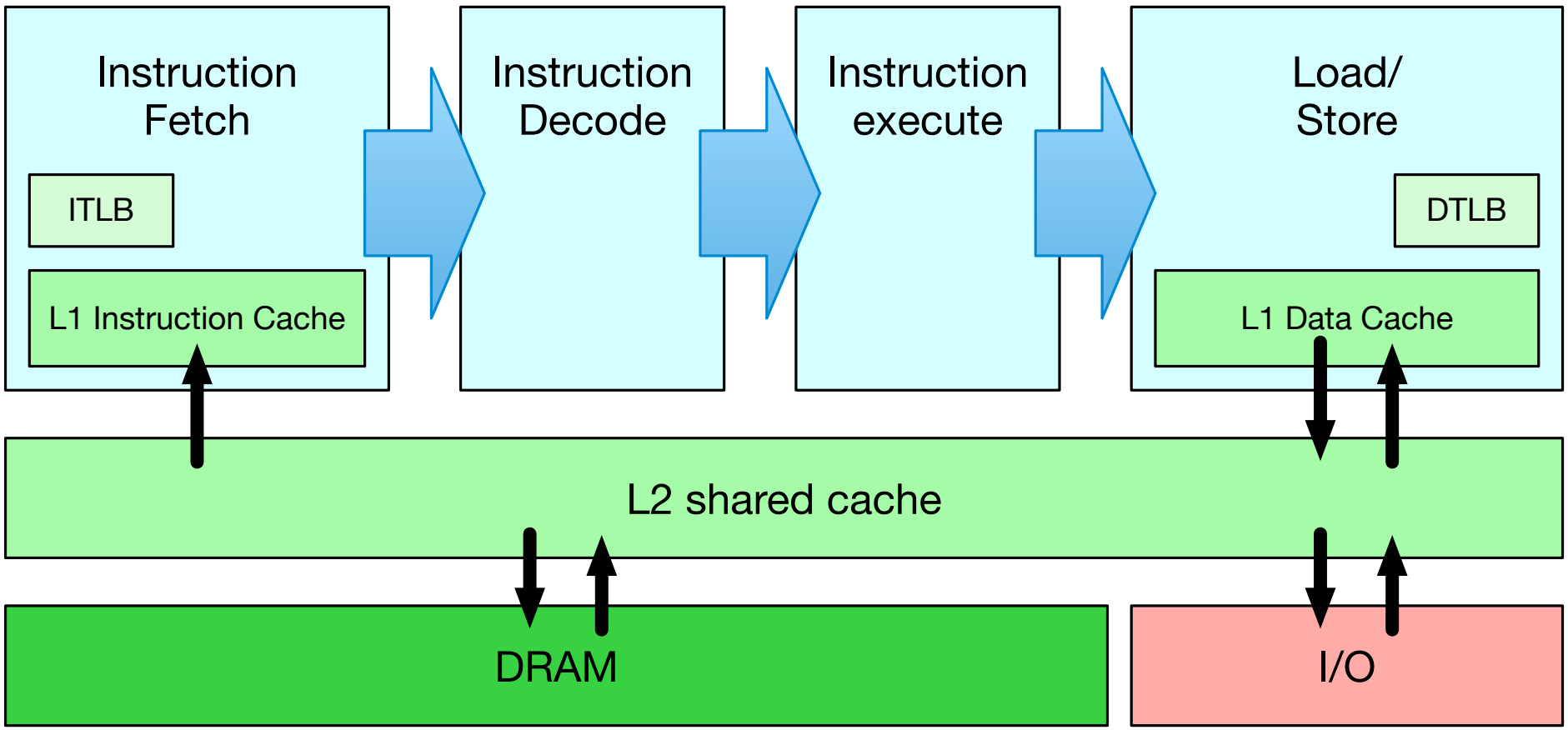
- Hardware performance counters
- Extending Lab 2 from OS effects to architecture/microarchitecture
- Updates to the IPC benchmark
- Gather further data for assessed *Lab Report 2*

Hardware performance counters

- Seems simple enough:
  - Source code compiles to instructions
  - Instructions are executed by the processor
- But some instructions take longer than others: multiply, etc
  - Optimisation is not just about reducing instruction count: some instructions matter more than others
  - More generally, hardware-level information can reveal where hardware-software interactions may be inefficient – e.g., poor utilisation of a cache or the TLB
- Hardware performance counters let us directly ask the processor about *architectural* and *microarchitectural* events
  - E.g., instruction count, memory accesses, cache-miss rate, AXI bus traffic to DRAM

Sketch of ARM Cortex A8 memory hierarchy



This is a very, very rough sketch indeed!

The benchmark – now with added PMC

```
root@beaglebone:/data/lab3 # ./ipc-static
ipc-static [-Bqsv] [-b buffersize] [-i pipe|socket]
  [-P l1d|l1i|l2|mem|tlb|axi] [-t totalsize] mode

Modes (pick one - default 1thread):
    1thread                 IPC within a single thread
    2thread                 IPC between two threads in one process
    2proc                   IPC between two threads in two different proces

Optional flags:
    -B                      Run in bare mode: no preparatory activities
    -i pipe|socket          Select pipe or socket for IPC (default: pipe)
    -P l1d|l1i|l2|mem|tlb|axi  Enable hardware performance counters
    -q                      Just run the benchmark, don't print stuff out
    -s                      Set send/receive socket-buffer sizes to buffers
    -v                      Provide a verbose benchmark description
    -b buffersize           Specify a buffer size (default: 131072)
    -t totalsize            Specify total I/O size (default: 16777216)
```

- New `-P` argument request profiling of load/store instructions, L1 D-cache, L1 I-cache, L2 cache, I-TLB, D-TLB, and AXI

Example: Profile memory instructions

```
root@beaglebone:/data/lab3 # ./ipc-static -vP mem -b 1048576 -i socket
  1thread
Benchmark configuration:
  buffersize: 1048576
  totalsize: 16777216
  blockcount: 16
  mode: 1thread
  ipctype: socket
  time: 0.084140708

  pmctype: mem
  INSTR_EXECUTED: 25463397
  CLOCK_CYCLES: 46233168
  CLOCK_CYCLES/INSTR_EXECUTED: 1.815672
  MEM_READ: 8699699
  MEM_READ/INSTR_EXECUTED: 0.341655
  MEM_READ/CLOCK_CYCLES: 0.188170
  MEM_WRITE: 7815423
  MEM_WRITE/INSTR_EXECUTED: 0.306928
  MEM_WRITE/CLOCK_CYCLES: 0.169044

194721.45 KBytes/sec
```

Example: Profile memory instructions

- Benchmark run pushed 16m data through a socket using 1m buffers for reads and writes
- Reasonable expectation of load and store memory footprints to be 16m $\times 2 + \epsilon$ reflecting copies to and from kernel buffers

- Word size in ARMv7 is 32 bits
- Memory reads (8,699,699) $\times$ 4 = $\approx$32M – sum of buffer accesses in user and kernel memory
- Could now query L1, L2 caches: how many of those accesses are in each cache, and how does it affect performance?

Exploratory questions

- How do requested memory access vary across our six benchmark configurations?
- How does varying the buffer size (and kernel socket-buffer size) impact L1, L2 cache effectiveness?
- In what situations might using a smaller buffer size to improve cache effectiveness hurt performance?

Experimental questions for lab report

- How does changing the IPC buffer size affect memory behaviour?
- Can we reach conclusions about the scalability of pipes vs. sockets?
- How does DTrace itself perturb the microarchitecture?

This lab session

- Upgrade your SD Card image (again)
  - This version has PMC improvements and further DTrace fixes
  - Ensure you've saved any scripts/data from your old card
  - You will need to reinstall your SSH key on the new SD card
  - Return the old card to us – we may provide future updates!
- Use this session to continue to build experience:
  - Build and use the updated IPC benchmark
  - Use PMC to analyse the benchmark
- Do ask us if you have any questions or need help