

SoC D/M Exercises 10/11

These exercises are allocated marks at Tripos examination level, with 20 marks making a full exam question. Example answers are available to supervisors. There is some repetition of material between the exercises, so a suitable target is to solve approximately half of them. Those marked with a heart (♥) are recommended.

1 ABD: Assertion-Based Design.

ABD1. ♥ : Assertion-based design.

- a) What is the difference between a safety and liveness assertion over the behaviour of a system. [4 Marks]
- b) How does a declarative safety assertion differ from an imperative assert statement ? [4 Marks]
- c) How can safety and liveness assertions be used in dynamic validation ? [5 Marks]
- d) Give a short segment of RTL or pseudocode that contains an imperative assertion that holds and give also a pair of valid safety and liveness assertions that hold for your code. [7 Marks]

ABD2. ♥ : Black & White Box Testing

Black-box testing is where the implementation details of a component are hidden and so assertions must be made about the observable behaviour at the ports of a component. White-box testing allows internal state to be monitored and reveals the next state function of the implementation.

Suppose a controller module has the following connections:

```
input clock;
input sensor_A;
input sensor_B;
output actuator_C;
output actuator_D;
```

- a) Give an example safety assertion that can potentially be used both with black and white-box testing. [4 Marks]
- b) Can your assertion be dynamically validated under black-box testing. [4 Marks]
- c) Can your assertion be formally proved under black-box testing. [4 Marks]
- d) Give an example liveness assertion that can potentially be used both with black and white-box testing. [4 Marks]
- e) Can your second assertion be dynamically validated under black-box testing. [4 Marks]
- f) Assuming a digital logic implementation of the controller, can your second assertion be formally proved under white-box testing. [4 Marks]

ABD3. : General ABD.

- a) What are the benefits of the assertion-based design (ABD) methodology ? [5 Marks]
- b) Illustrate how a regular expression can be used as part of a safety assertion ? [5 Marks]
- c) Using three or more *modelling layers*, describe the PSL reference model. [5 Marks]

In PSL next-cycle suffix implication uses $|=>$ and same-cycle suffix implication uses $|->$.

- d) Use these two different forms to give a pair of PSL expressions that have identical meaning. [6 Marks]

See http://www.esperan.com/tutorial/psl_simple.html

ABD4. Four-phase handshake.

- a) Give a temporal logic expression that defines a four-phase handshake using PSL or a PSL-like language. [12 Marks]
- b) Give the synthesisable RTL, SystemC or circuit for a monitor that checks operation of a four-phase handshake. You may assume a high-frequency clock is available that does not alias any transitions. (*Hint: an answer to this is, this-year, in the toyclasses folder.*) [6 Marks]
- c) What is automated stimulus generation and consider whether it be practically applied to interfaces such as the four-phase H/S? [3+3 Marks]

ABD5. ♡ : Protocol, Interface and Bus Monitors.

- a) What is meant by the terms ‘port’ and ‘interface’ ? [4 Marks]
- b) What is meant by the formal specification of a protocol and what is a bus monitor ? [5 Marks]
- c) How are bus monitors used in ABD and what sort of error might be detected (safety of liveness etc.) ? [5 Marks]
- d) How can a bus monitor be used to generate simulation stimulus ? What coverage might be possible ? [5 Marks]
- e) What statistics might a bus monitor collect ? [5 Marks]

ABD6. : PSL Operators and Algorithm.

- a) Why is it recommended to always use a PSL SERES as part of a suffix implication ? [5 Marks]
- b) Describe five infix operators defined in PSL. [5 Marks]
- c) Outline an algorithm for synthesising a pattern detecting automaton from the main operators in a PSL SERES (regular expression). (*This was not lectured in 09/10 but is briefly included in the additional material. In 10/11 some ML fragments were flashed up. Candidates ought to be able to do this from Ia RL&FSA material: it’s a core competence.*) [5 Marks]

ABD7. : ABD Methodology.

- a) What is meant by ‘Assertion Based Design’ ? [5 Marks]
- b) Compare the use of assertions and yes/no test wrappers in regression testing ? [5 Marks]
- c) Explain how certain assertions can be re-used at different layers of modelling abstraction (and others not). For example, some might be used for TLM modelling as well as for pre-synthesis and post-synthesis forms of an RTL design. [5 Marks]
- d) What is meant in testing by the term ‘coverage’ and can this be applied to set of assertions ? [5 Marks]

ABD8. : Sequential Equivalence Checker (SEC).

- a) What is the combinational equivalence problem ? What is the role of don’t cares in it ? [5 Marks]
- b) What is meant by sequential equivalence and strong and weak/stuttering bi-simulation ? [5 Marks]
- c) Why might sequential equivalence be violated in a design flow (i.e. SEC gives a negative result)? [5 Marks]
- d) Why might we see false negatives from a SEC ? [5 Marks]