MPhil in Advanced Computer Science
System On Chip Design and Modelling : 2010/11

Leader:	Dr David Greaves
Timing:	Lent
Prerequisites:	Some experience with VHDL/Verilog RTL, Assembler, C++
Structure:	8 lectures + 8 practicals/coursework: and research project option.

AIMS

A current-day system on a chip (SoC) consists of several different microprocessor subsystems together with memories and I/O interfaces. This course covers SoC design and modelling techniques with emphasis on architectural exploration, assertion-driven design and the concurrent development of hardware and embedded software. This is the 'front end' of the design automation tool chain. (Back end material, such as design of individual gates, layout, routing and fabrication of silicon chips is not covered.)

SYLLABUS

All candidates must have a basic knowledge of programming, digital hardware and assembly language programming. Experience with C++ is also highly useful.

1. **Low-level Modelling and Design Refactoring**

   Verilog RTL Design with examples. Simulation styles (fluid flow versus eventing). Basic RTL to gates synthesis algorithm. Using signals, variables and transactions for component inter-communication. SystemC overview. Structural hazards, retiming, refactoring.

2. **Design Partition, High-level and Hybrid Modelling.**

   Bus and cache structures, DRAM interface. SoC parts. Design exploration. Hardware/software interfaces and co-design. Memory maps. Programmer's model. Firmware development. Transactional modelling. Electronic systems level (ESL). IP-XACT. Instruction set simulators, cache modelling and hybrid models.

3. **Assertions for Design, Testing and Synthesis.** Assertion based design: testing and synthesis. PSL/SVA assertions. Temporal logic compilation to FSM. Glue logic synthesis. Combinational and sequential equivalence. High-level Synthesis and Automated Assembly.

4. **Power Control and Power Modelling.** Power consumption formulae. Pre-layout wiring estimates. Clock gating. Frequency and voltage dynamic scaling.

OBJECTIVES

On completion of this module students should:

- be familiar with how complex gadgets, containing multiple processors, such as an iPod or a sat-nav are designed and developed.
- understand the hardware and software structures used to implement and model inter-component communication in such devices,
- be fully familiar with SystemC including transactional modelling,
- have basic experience using temporal logic and assertions,
- have designed a SoC architecture at a high level of abstraction, to have run at least one application on it and to have studied its power consumption.

COURSEWORK

The students will attend eight afternoon sessions where they at first repeat demos developed in the lectures and later develop their own version of a SoC in larger, team-based projects. The initial exercise uses Verilog RTL, but everything else is done using SystemC/TLM (GCC/linux). We use a SystemC multi-processor model using a loosely-timed transactional bus model. This, itself, runs Splash benchmarks, user embedded applications and optionally linux. Students can alter the number of cores and bus and cache structures or add their own hardware models, while exploring the power consumption for their chosen embedded operating system and/or application hosted on the SoC.

RESEARCH PROJECT

The coursework itself contains a lot of practical project work and this is easy to extend in any relevant direction. Alternatively, the modelling tools could be extended in new directions, such as implementing very-high-level simulation or new new logic synthesis algorithm recently reported in the literature. Very-high-level simulation is a new area, where power estimates and other metrics of interest, such as chip area, are obtained from broad-brush design partition decisions without resorting to detailed implementation.

MODULE TIME BUDGET

- 16 SW02 sessions,
- 4 post session supervisions,
- 20 private study,
- 15 coursework exercises, mini-project I and other ticks (excluding additional time during classes),
- 25 mini-project II & Research Essay (easter vacation).

This is a total of 80 hours split over the Lent term and (for mini-project II) over the Easter break.

ASSESSMENT

- The lectured component is assessed with a combination of written exercises and small-scale practical projects This accounts for 50 percent of the course credit.
- Over the Easter vacation, students must complete a SoC design (based on integrating some of the smaller projects already completed) and a research essay (entitled 'SoC Design and Modelling') which together account for the second 50 percent of the course credit.

RECOMMENDED READING

'*Transaction-Level Modeling with SystemC: TLM Concepts and Applications for Embedded Systems*' by Frank Ghenassia. Published Springer 2010.
'*System Design with SystemC*', Springer. Grotket, Liao, Martin and Swan.
'*SystemC tutorials and whitepapers.*' Download from OSCI www.systemc.org
'*Essential Issues in SoC Design: Designing Complex Systems-on-chip*', Spinger. Youn-Long Steve Lin (Editor).

Last updated: September 2010