MPhil in Advanced Computer Science
Chip Multiprocessors

Leader:	Robert Mullins
Timing:	Michaelmas
Prerequisites:	A good understanding of the fundamentals of computer architecture and some knowledge of VLSI design.
Structure:	8 x two-hour seminars

AIMS

This course aims to provide an introduction to parallel computing with a particular focus on chip multiprocessors. The course begins by examining the motivation for the current shift away from uniprocessors. It explores the basics of parallel algorithm design, approaches to parallel programming and the architecture of modern chip-multiprocessors. The final seminar explores the challenges in attempting to scale chip-multiprocessor designs beyond the modest number of cores seen in today's designs.

SYLLABUS

1. Trends in microprocessor architecture
2. Introduction to parallel computing
3. Parallel algorithms
4. Chip multiprocessor architecture and cache coherency (2 seminars)
5. Transactional memory
6. On-chip interconnection networks
7. Manycore research issues

OBJECTIVES

On completion of this module students should:

- understand the reasons for the shift from wide-issue superscalar to multi-core processors.
- appreciate the challenges involved in exploiting parallel processors and their limits.
- be familiar with a range of approaches to parallel programming based on both shared-memory and message-passing models
- understand the cache-coherency and transactional memory systems that support shared-memory programming in multiprocessors

- have a clear understanding of the wide range of possible on-chip interconnection network designs.
- be able to discuss the challenges in exploiting a large number (possibly hundreds) of processing cores on a single chip.

COURSEWORK

To complete two paper reviews and write a short survey paper.

ASSESSMENT

Each seminar will consist of a short lecture, reading club and student presentations. Assessments will be set and marked by the course lecturer.

- Test (50%)
- Coursework and ticks (50%)
  (10% for each review, 20% for survey paper, 10% for participation)
- Final module mark will be percentage.

RECOMMENDED READING

Culler, D. E. and Singh, J. P. (1999) *Parallel Computer Architecture: A Hardware/Software approach*, Morgan Kaufmann, ISBN 1-55860-343-3
Grama, A, Anshul, G., Karypis, G and Kuman, V. (2004) *Introduction to Parallel Computing*, Addison-Wesley (2nd Edition)
Hennessy, J. L. and Patterson, D. A. (2006). *Computer Architecture: A Quantitative Approach"* Morgan Kaufmann (4th Edition)
Herlihy, M. and Sahvit, N. (2008) *The art of multiprocessor programming*, Morgan Kaufmann, ISBN: 978-0-12-370591-4
Olukotun, K., Hammond, L. and Laudon, J. (2007) *Chip Multiprocessor Architecture*, Morgan Claypool, ISBN: 978-1598291223

A list of papers will also be provided for discussion at each seminar. The complete reading list will be available from the course web page.

Preparatory reading:
All students should have a good knowledge of the material presented in the Hennessy and Patterson book. Chapter 4. in particular is essential reading before the course begins.

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