NetFPGA Summer Course

Presented by:

Noa Zilberman

Yury Audzevich

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http://NetFPGA.org

The secret recipe for a working simulation

1. source tools/settings.sh
2. source /opt/Xilinx/Vivado/2014.4/settings64.sh
3. make
4. cd $NF_DESIGN_DIR/hw
5. make reg
6. cd local_ip
7. mv crypto crypto_v1_0_0
8. cd crypto_v1_0_0
9. vi Makefile ,edit line 29: vivado -mode batch -source crypto.tcl
10. mv example.tcl crypto.tcl
11. vi crypto.tcl ,edit line 57: read_verilog "./hdl/crypto.v"
12. cd hdl
13. mv example.v crypto.v
14. vi crypto.v
15. change module name to “crypto”
16. cd $NF_DESIGN_DIR/hw
17. make core
18. cd $SUME_FOLDER/tools/scripts
19. ./nf_test.py sim --major crypto --minor test

make core going wild

CRITICAL WARNING: [filemgmt 20-742] The top module "crypto" specified for this project can not be validated. The current project is using automatic hierarchy update mode, and hence a new suitable replacement top will be automatically selected. If this is not desired, please change the hierarchy update mode to one of the manual compile order modes first, and then set top to any desired value.

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ERROR: [filemgmt 20-730] Could not find a top module in the fileset sources_1.

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You've got syntax errors!!!

Start by checking ports and parameters syntax