A Priori System-Level Interconnect Prediction
Rent’s Rule and Wire Length Distribution Models

Dirk Stroobandt
Ghent University
Electronics and Information Systems Department

Tutorial at SLIP 2001
March 31, 2001
Outline

Why a priori interconnect prediction?
Basic models
Rent’s rule
A priori wire length prediction
Recent advances
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Why A Priori Interconnect Prediction?

• **Interconnect**: importance of wires increases (they do not scale as components).
• **A priori**:
  • For future designs, very little is known.
  • The sooner information is available, the better.
• A Priori Interconnect Prediction = estimating interconnect properties and their consequences before any layout step is performed.
• Extrapolation to future systems: Roadmaps.
• To improve CAD tools for design layout generation.
• To evaluate new computer architectures.
Why A Priori Interconnect Prediction?

- Extrapolation to future systems:
  - Roadmaps.
  - GTX* et al.

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Why A Priori Interconnect Prediction?

• To improve CAD tools for design layout generation.

More efficient layout generation requires good wire length estimates.
• layer assignment in routing
• effects of vias, blockages
• congestion, ...

A priori estimates are rough but already provide a better solution through fewer design cycle iterations.
Why A Priori Interconnect Prediction?

To evaluate new computer architectures

OIIC Project (http://www.elis.rug.ac.be/~jvc/oiic/sysdemo.htm)
Goal: Predict Interconnect Requirements vs. Resource Availability
Setting of SLIP Research Domain in the Design Process

1. Circuit design
2. Physical design
3. Fabrication
Components of the Physical Design Step

- Circuit
- Architecture
- Layout generation
- Layout
The Three Basic Models

Circuit model

Model for the architecture

- Cell
- Pad
- Channel

Manhattan grid using Manhattan metric

\[ d = |x_1 - x_2| + |y_1 - y_2| \]

Placement and routing model
Outline

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Rent’s Rule

Rent’s rule was first described by Landman and Russo* in 1971. For average number of terminals and blocks per module in a partitioned design:

\[ T = t B^p \]

\( p = \text{Rent exponent} \)

\( t \approx \text{average } \# \text{ term./block} \)

Measure for the complexity of the interconnection topology
Intrinsic Rent exponent \( p^* \)
(simple) \( 0 \leq p^* \leq 1 \) (complex)

Normal values: \( 0.5 \leq p^* \leq 0.75 \)

Rent’s Rule (cont.)

Rent’s rule is a result of the self-similarity within circuits.

Assumption: the complexity of the interconnection topology is equal at all levels.
Rent’s Rule (other definition)

(Dense) region: B cells, T terminals

If $\Delta B$ cells are added, what is the increase $\Delta T$?
In the absence of any other information we guess

$$\Delta T = \left(\frac{T}{B}\right)\Delta B$$

Overestimate: many of $\Delta T$ terminals connect to $T$ terminals and so do not contribute to the total.

We introduce* a factor $p$ ($p < 1$) which indicates how self-connected the netlist is + placement optimization

$$\Delta T = p\left(\frac{T}{B}\right)\Delta B$$

Or, if $\Delta B$ & $\Delta T$ are small compared to $B$ and $T$

$$\frac{dT}{T} \approx p\left(\frac{dB}{B}\right) \Rightarrow T = tB^p$$

Rent’s Rule (summary)

\[ T = t B^p \]

Rent’s rule is experimentally validated for a lot of benchmarks.

Distinguish between:
- \( p^* \): intrinsic Rent exponent
- \( p \): placement Rent exponent
- \( p' \): partitioning Rent exponent

Deviation for high \( B \) and \( T \):
Rent’s region II*

Also: deviation for low \( B \) and \( T \):
Rent region III**


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Donath’s* Hierarchical Placement Model

1. **Partition the circuit** into 4 modules of equal size such that Rent’s rule applies (minimal number of pins).

2. **Partition the Manhattan grid** in 4 subgrids of equal size in a symmetrical way.

Donath’s Hierarchical Placement Model

3. Each subcircuit (module) is mapped to a subgrid.

4. Repeat recursively until all logic blocks are assigned to exactly one grid cell in the Manhattan grid.
Donath’s Length Estimation Model

At each level: Rent’s rule gives number of connections

- number of terminals per module directly from Rent’s rule (partitioning based Rent exponent $p'$);
- number of nets cut at level $k$ ($N_k$) equals

$$N_k = \alpha T_k$$

where $\alpha$ depends on the total number of nets in the circuit and is bounded by 0.5 and 1.
Donath’s Length Estimation Model

Length of the connections at level $k$?

Donath assumes: all connection source and destination cells are uniformly distributed over the grid.
Scaling of the average length $L$ as a function of the number of logic blocks $G$:

$$L \propto \begin{cases} 
G^{p-0.5} & (p > 0.5) \\
\log(G) & (p = 0.5) \\
f(p) & (p < 0.5)
\end{cases}$$

Similar to measurements on placed designs.
Theoretical average wire length too high by factor of 2
Improving on the Placement Optimization Model

- Keep **wire length scaling** by hierarchical placement.
- Improve on **uniform probability** for all connections at one level (not a good model for placement optimization).

*Occupation probability* favours short interconnections (for placement optimization) (darker)

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Including Placement Optimization

Wirelength distributions contain two parts:

1. site density function
2. probability distribution

All possibilities require enumeration (use generating polynomials*).

Probability of occurrence:

\[ N(l) = K D(l) q(l) \]

Occupation Probability Function

Local distributions at each level have similar shapes (self-similarity) ⇒ peak values scale.
Integral of local distributions equals number of connections.
Global distribution follows peaks.

From this we can deduce that

\[ N(l) \propto l^{2p-3} \]

For short lengths: \[ D(l) \propto l \]

\[ \Rightarrow q(l) \propto \frac{N(l)}{D(l)} \propto l^{2p-4} \]
**Occupation Probability Function**

Same result found by using a terminal conservation technique*

\[
N_{A\rightarrow C} = \alpha T_{A\rightarrow C} = \alpha \left[ (1 + B_B)^p + (B_B + B_C)^p - B_B^p - (1 + B_B + B_C)^p \right]
\]


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Occupation Probability Function

For cells placed in infinite 2D plane

\[ B_C = 4l \]
\[ B_B = \sum_{l'=1}^{l-1} 4l' = 2l(l - 1) \]

\[ N_{A\rightarrow C} = \alpha t \left[ (1 + 2l(l - 1))^p + (2l(l - 1) + 4l)^p - (2l(l - 1))^p - (1 + 2l(l - 1) + 4l)^p \right] \]

\[ q(l) = \frac{N_{A\rightarrow C}}{4l} \propto l^{2p-4} \]
Occupation Probability: Results

Use probability on each hierarchical level (local distributions).

![Graph showing occupation probability, Donath, and experiment results.](image)
Occupation Probability: Results

Effect of the occupation probability: boosting the local wire length distributions (per level) for short wire lengths

![Graphs showing the effect of occupation probability on wire length distributions.](attachment:image.png)
Effect of the occupation probability on the total distribution: more short wires = less long wires

⇓

Average wire length is shorter

Occupation Probability: Results

Donath
Occupation prob.
Occupation Probability: Results

![Graph showing occupation probability results. The x-axis represents wire length ranging from 1 to 10, and the y-axis represents percent wires ranging from 0 to 60. The graph includes three lines: Donath (red), Occupation prob. (green), and Global trend (blue).]

-8%  -23%  +10%  +6%
Occupation Probability: Results

Number of wires

Wire length

Donath
Occupation prob.
Measurement
Outline

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Length of Multi-terminal Nets

Difference between delay-related and routing-related applications*:

- **Source-sink pairs**
  
  Assume A is source
  
  A-B at level \( k \)
  
  A-C and A-D at level \( k + 1 \)
  
  **Count as three connections**

- **Entire Steiner tree lengths**
  
  Segments A-B, C-D and E-F
  
  A-B and C-D at level \( k \)
  
  E-F at level \( k + 1 \)
  
  **Add lengths to one net length**

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Extension to Three-dimensional Grids*


Anisotropic Systems*

Anisotropic Systems

Not all dimensions are equal (e.g., optical links in 3rd D)

- Possibly larger latency of the optical link (compared to intra-chip connection);
- Influence of the spacing of the optical links across the area (detours may have to be made);
- Limitation of number of optical layers

Introducing an **optical cost**
External Nets

Importance of good wire length estimates for external nets* during the placement process:

For highly pin-limited designs: placement will be in a ring-shaped fashion (along the border of the chip).

Wire Lengths at System Level

At system level: many long wires (peak in distribution).

How to model these?

Estimation* based on Rent’s rule with the floorplanning blocks as logic blocks.

Conclusion

Wire length distribution estimations have evolved a lot in the last few years and have gained accuracy but the work is not finished!

Suggested reading (brand new book):

D. Stroobandt.
A Priori Wire Length Estimates for Digital Design.
ISBN no. 0 7923 7360 x.