A Priori System-Level Interconnect Prediction

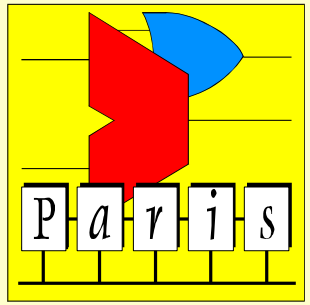
Rent's Rule and Wire Length Distribution Models

Dirk Stroobandt

Ghent University
Electronics and Information Systems Department

UNIVERSITEIT GENT
Elektronica en Informatiesystemen

Tutorial at SLIP 2001
March 31, 2001



Outline

Why a priori interconnect prediction?

Basic models

Rent's rule

A priori wire length prediction

Recent advances

Outline

Why a priori interconnect prediction?

Basic models

Rent's rule

A priori wire length prediction

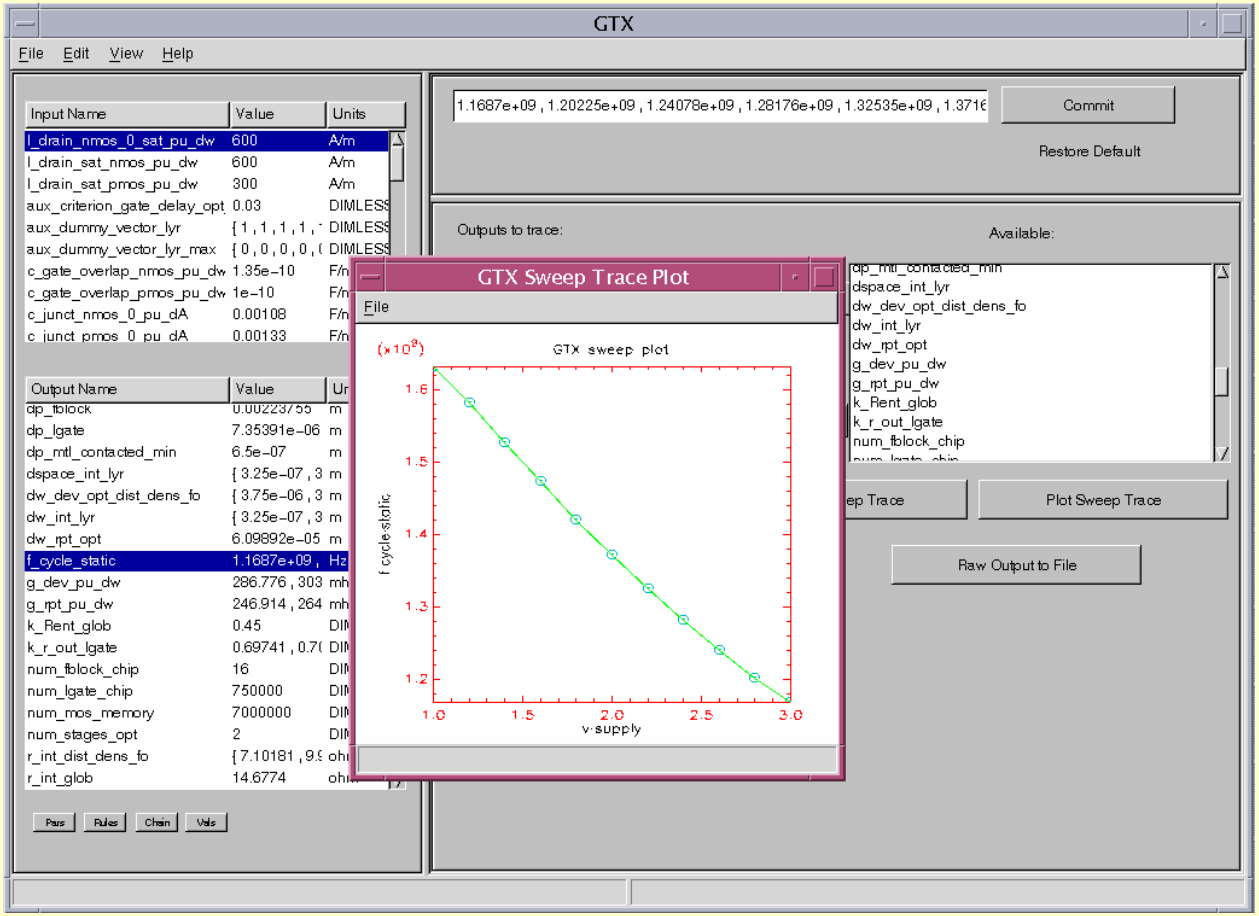
Recent advances

Why A Priori Interconnect Prediction?

- *Interconnect*: importance of wires increases (they do not scale as components).
- *A priori*:
  - For future designs, very little is known.
  - The sooner information is available, the better.
- A Priori Interconnect Prediction = estimating interconnect properties and their consequences before any layout step is performed.
- Extrapolation to future systems: Roadmaps.
- To improve CAD tools for design layout generation.
- To evaluate new computer architectures.

Why A Priori Interconnect Prediction?

- Extrapolation to future systems:
  - Roadmaps.
  - GTX* et al.



* A. Caldwell et al. “GTX: The MARCO GSRC Technology Extrapolation System.” *IEEE/ACM DAC*, pp. 693-698, 2000 (http://vlsicad.cs.ucla.edu/GSRC/GTX/).

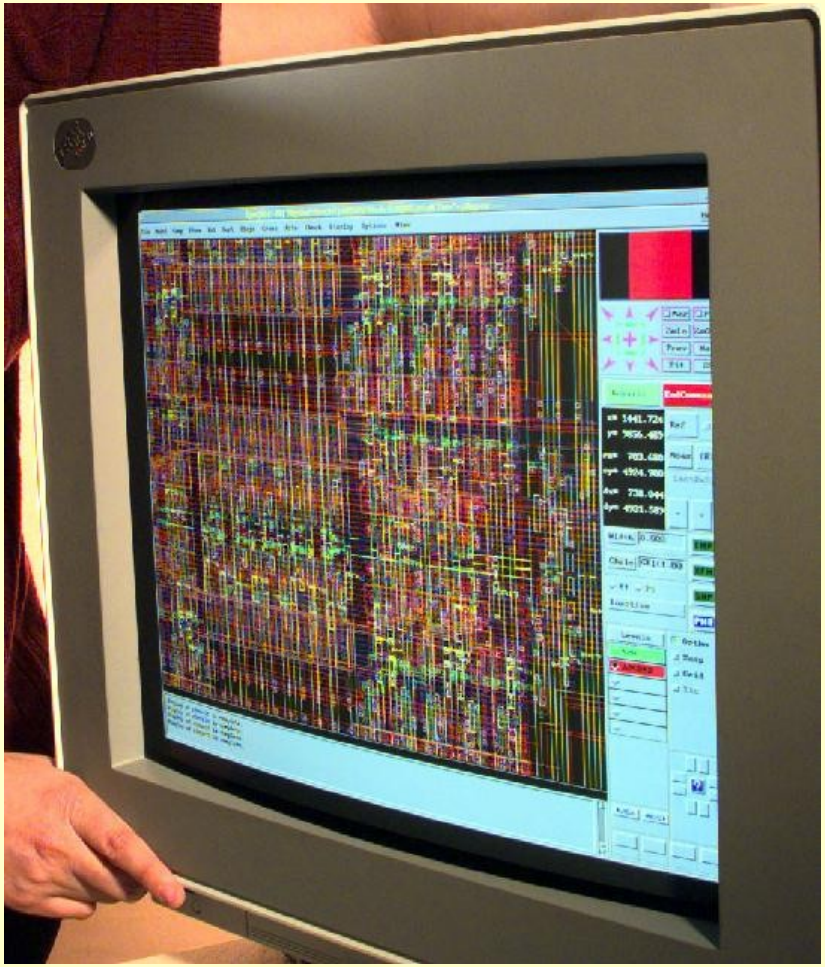
Why A Priori Interconnect Prediction?

- To improve CAD tools for design layout generation.

More efficient layout generation requires good wire length estimates.

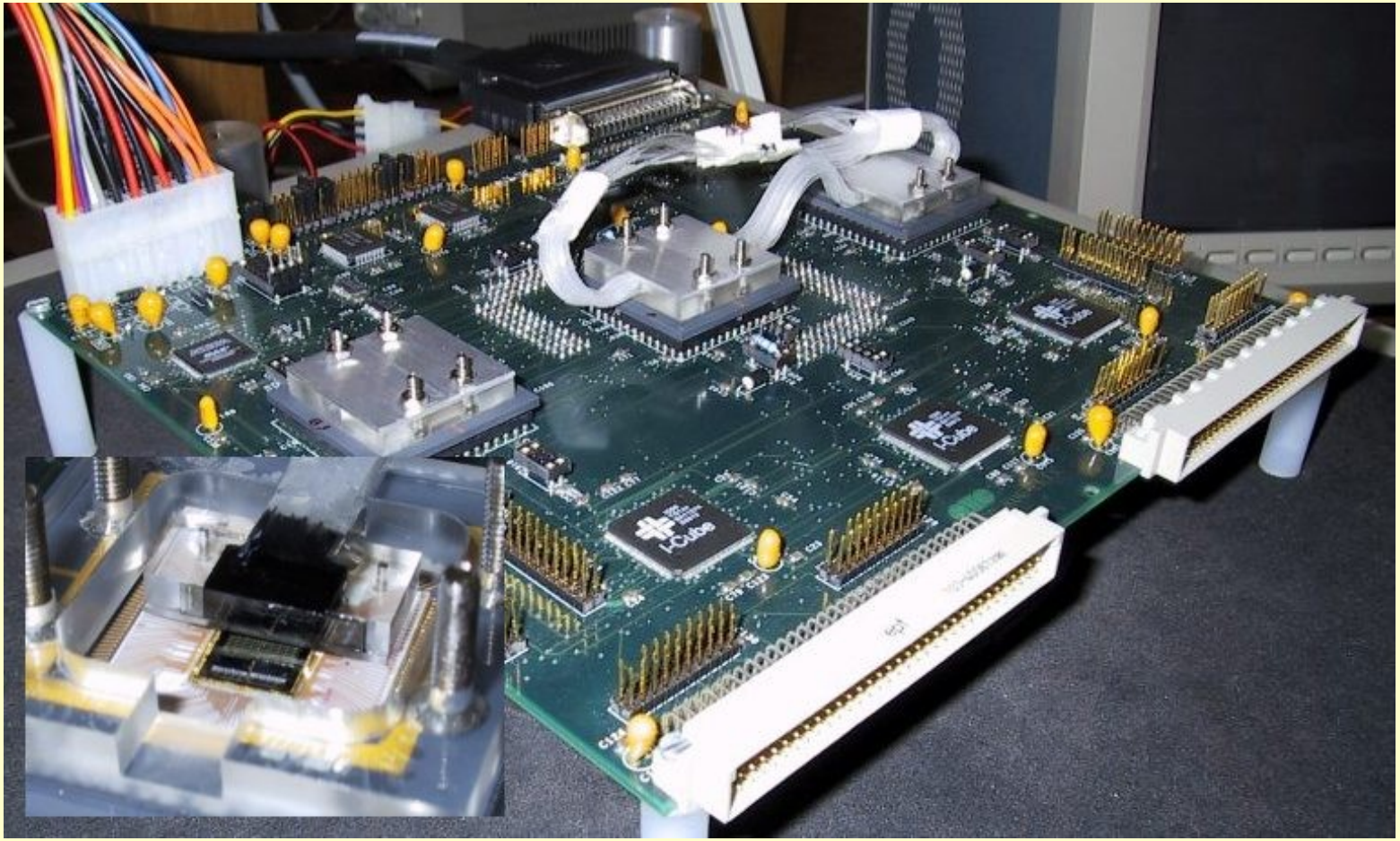
- layer assignment in routing
- effects of vias, blockages
- congestion, ...

A priori estimates are rough but already provide a better solution through fewer design cycle iterations.



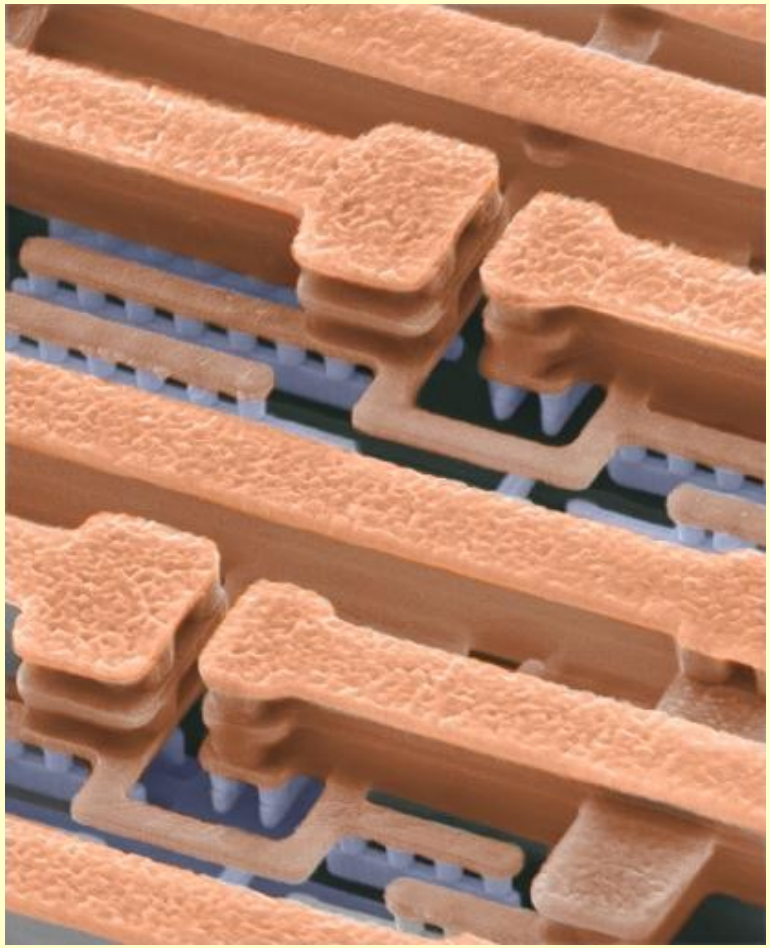
Why A Priori Interconnect Prediction?

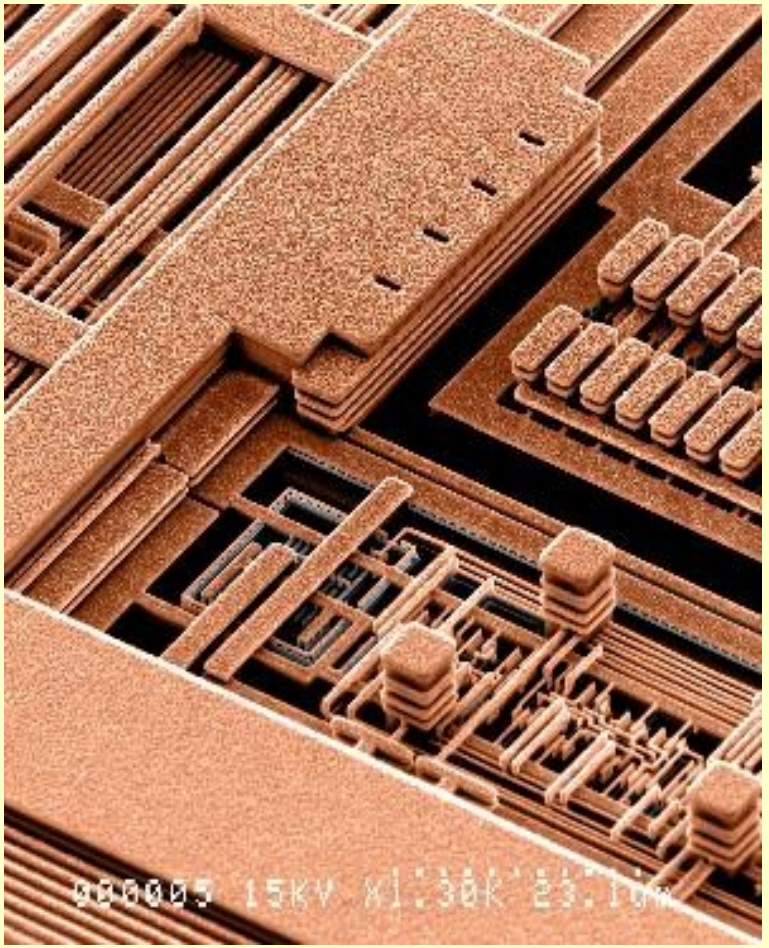
To evaluate new computer architectures



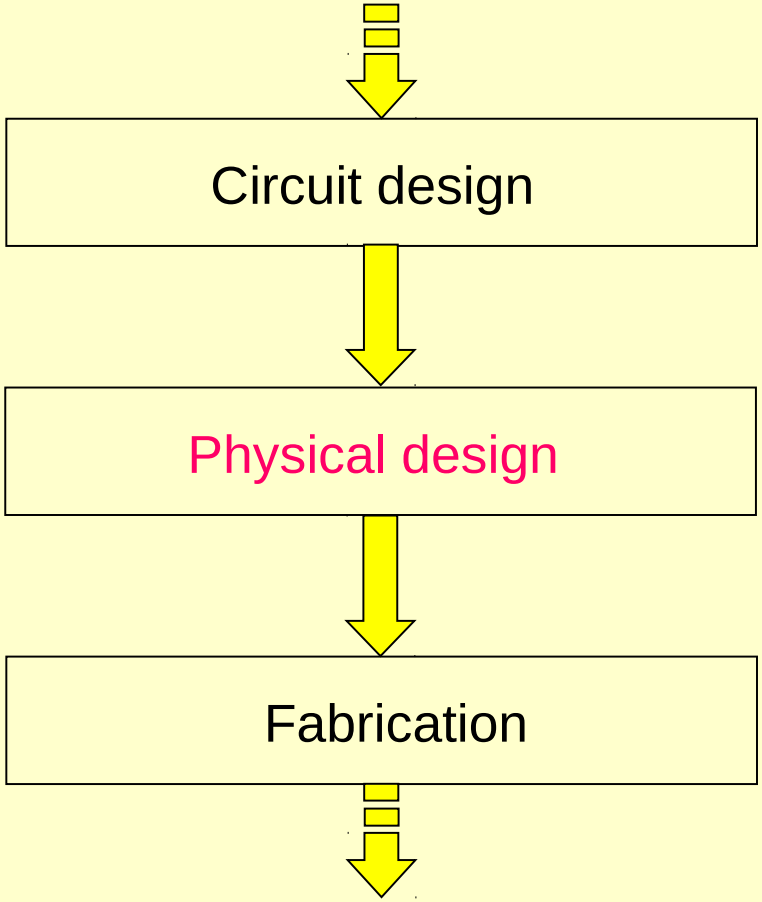
OIIC Project (http://www.elis.rug.ac.be/~jvc/oiic/sysdemo.htm)

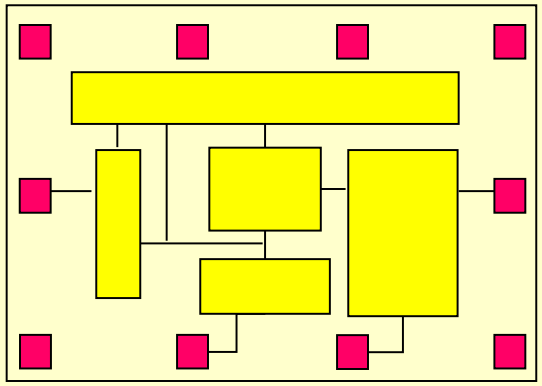
Goal: Predict Interconnect Requirements vs. Resource Availability



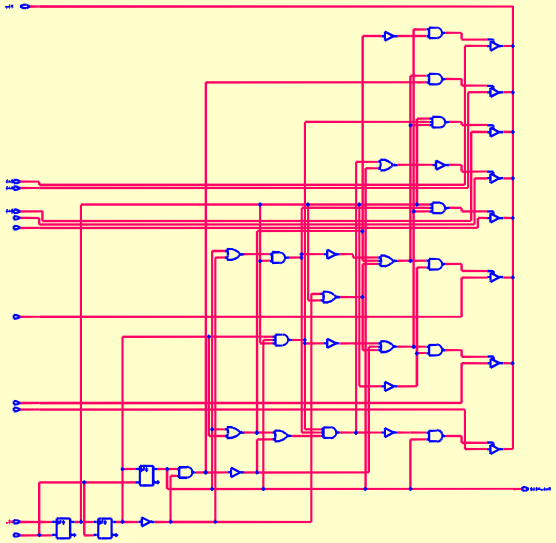


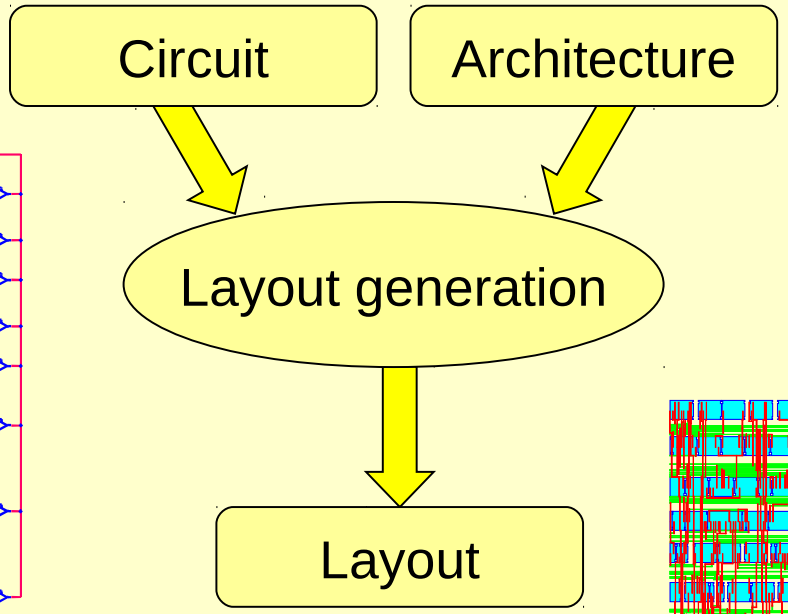
Setting of SLIP Research Domain in the Design Process

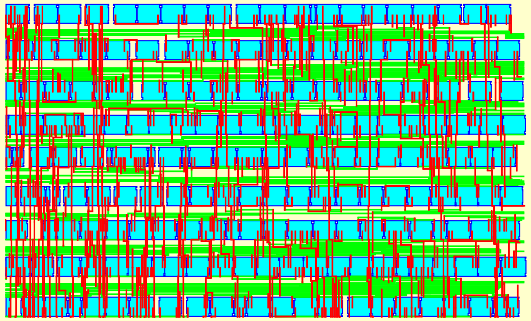




Components of the Physical Design Step



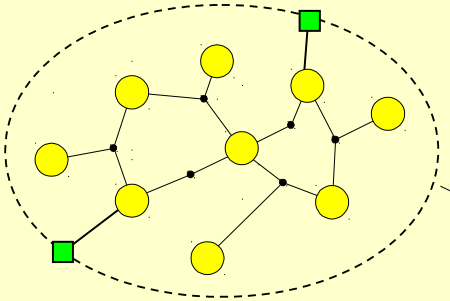


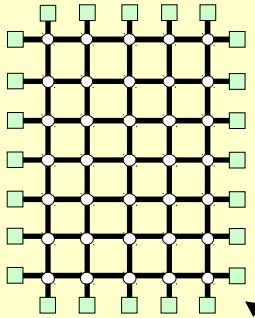


The Three Basic Models

Circuit model

Model for the architecture





Cell

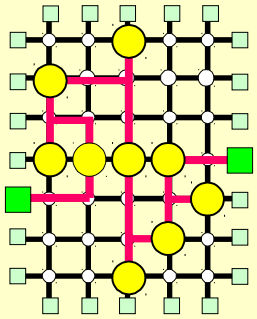
Pad

Channel

Logic block

Net

Terminal / pin



Manhattan grid
using Manhattan metric

$$d = | x_1 - x_2 | + | y_1 - y_2 |$$

Placement and routing model

Outline

Why a priori interconnect prediction?

Basic models

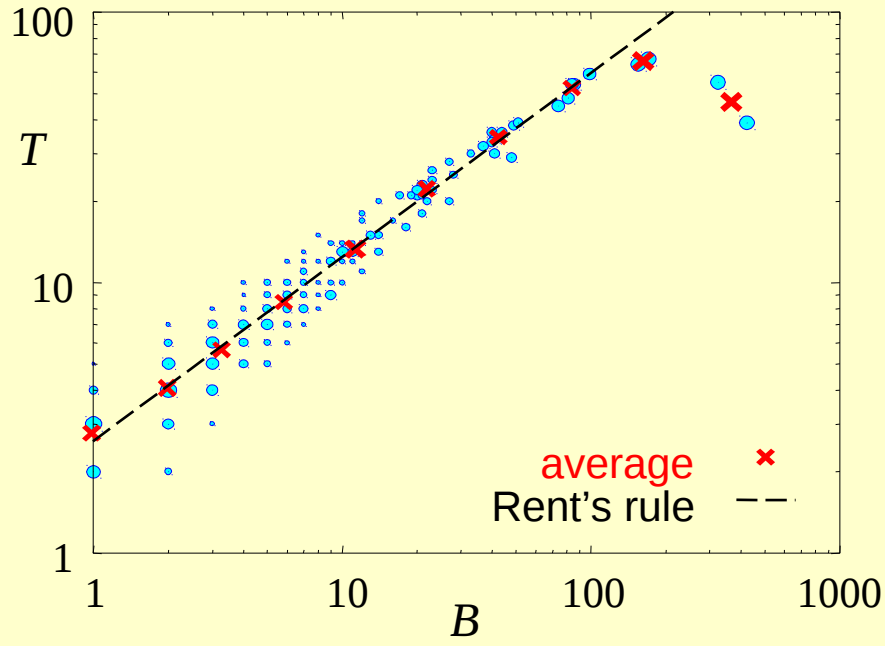
Rent's rule

A priori wire length prediction

Recent advances

Rent's Rule

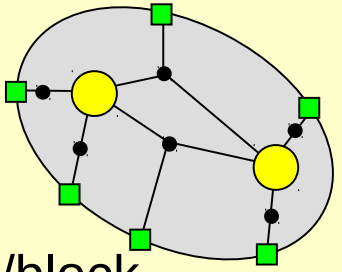
Rent's rule was first described by Landman and Russo* in 1971. For average number of terminals and blocks per module in a partitioned design:



$$T = t\,B^{p}$$

p = Rent exponent

$t \cong$ average # term./block



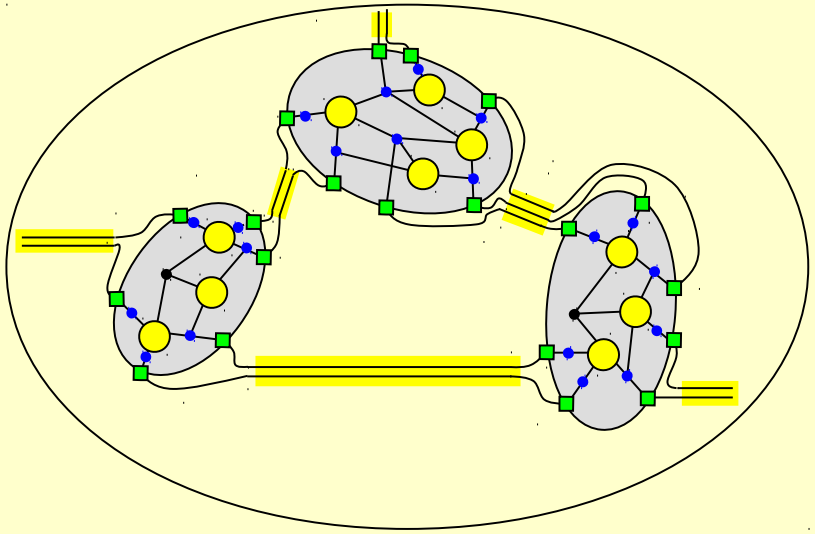
Measure for the complexity of the interconnection topology
Intrinsic Rent exponent p^*
(simple) $0 \le p^* \le 1$ (complex)

Normal values: $0.5 \le p^* \le 0.75$

* B. S. Landman and R. L. Russo. "On a pin versus block relationship for partitions of logic graphs." *IEEE Trans. on Comput*., C-20, pp. 1469-1479, 1971.

Rent's Rule (cont.)

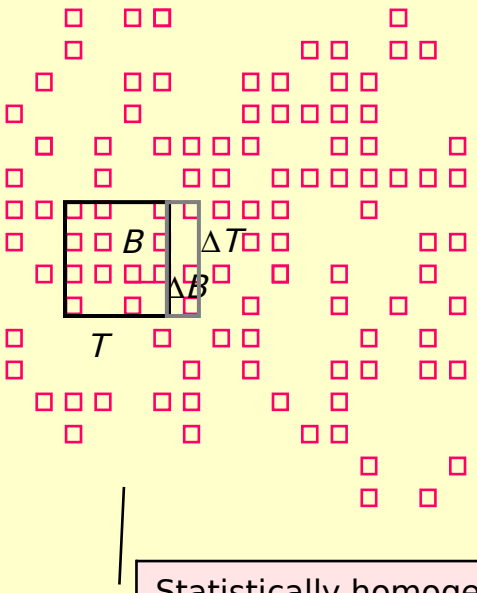
Rent's rule is a result of the self-similarity within circuits



Assumption: the complexity of the interconnection topology is equal at all levels.

Rent's Rule (other definition)

(Dense) region: B cells, T terminals



Statistically homogenous system

$$p^* \le p \le 1$$

If ΔB cells are added, what is the increase ΔT?
In the absence of any other information we guess

$$\Delta T = \left(\frac{T}{B}\right)\Delta B$$

Overestimate: many of ΔT terminals connect to T terminals and so do not contribute to the total.
We introduce* a factor ***p*** (***p*** <1) which indicates how self-connected the netlist is + placement optimization

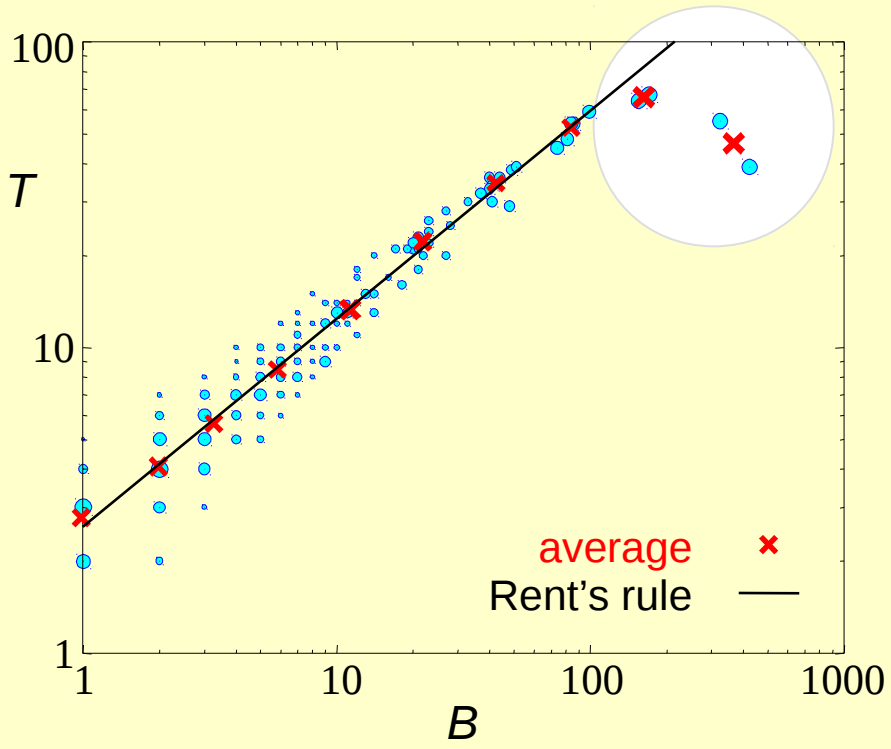
$$\Delta T = p\left(\frac{T}{B}\right)\Delta B$$

Or, if ΔB & ΔT are small compared to B and T

$$\frac{dT}{T} \approx p\left(\frac{dB}{B}\right) \Rightarrow T = tB^p$$

* P. Christie and D. Stroobandt. "The Interpretation and Application of Rent's Rule." *IEEE Trans. on VLSI Systems, Special Issue on SLIP*, vol. 8 (no. 6), pp. 639-648, Dec. 2000.

Rent's Rule (summary)



$$T = t\,B^{p}$$

Rent's rule is experimentally validated for a lot of benchmarks.

Distinguish between:
- *p**: intrinsic Rent exponent
- *p*: placement Rent exponent
- *p'*: partitioning Rent exponent

Deviation for high *B* and *T*:
Rent's region II*
Also: deviation for low *B* and *T*:
Rent region III**

* B. S. Landman and R. L. Russo. "On a pin versus block relationship for partitions of logic graphs." *IEEE Trans. on Comput*., C-20, pp. 1469-1479, 1971.

** D. Stroobandt. "On an efficient method for estimating the interconnection complexity of designs and on the existence of region III in Rent's rule." *Proc. GLSVLSI*, pp. 330-331, 1999.

Outline

Why a priori interconnect prediction?

Basic models

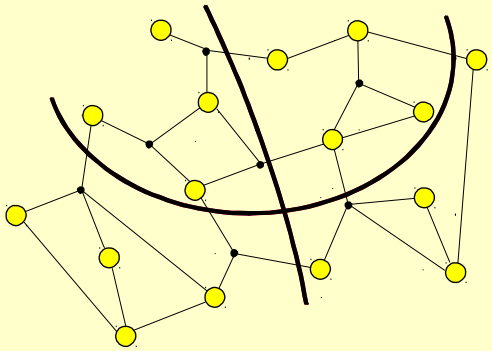
Rent's rule

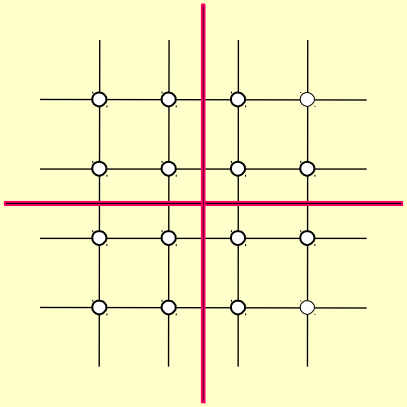
A priori wire length prediction

Recent advances

Donath's* Hierarchical Placement Model

1. Partition the circuit into 4 modules of equal size such that Rent's rule applies (minimal number of pins).



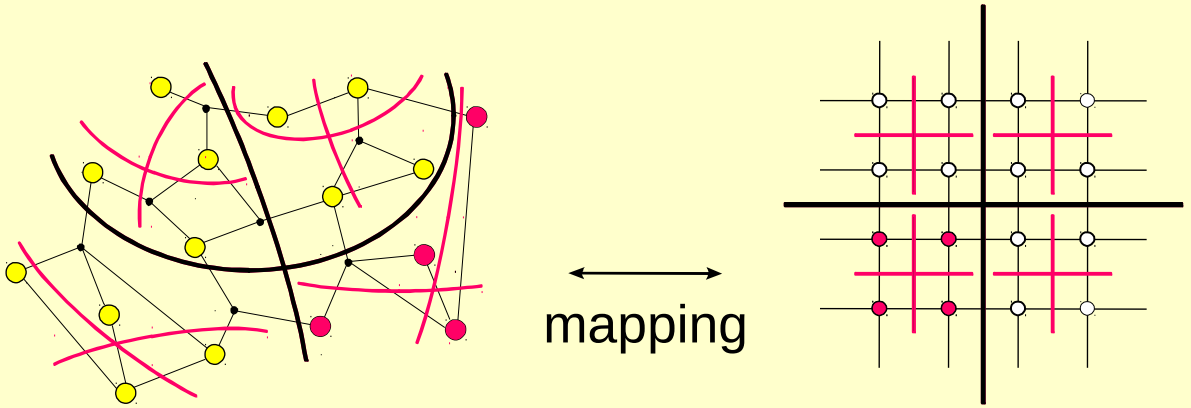


2. Partition the Manhattan grid in 4 subgrids of equal size in a symmetrical way.

* W. E. Donath. Placement and Average Interconnection Lengths of Computer Logic. *IEEE Trans. on Circuits & Syst*., vol. CAS-26, pp. 272-277, 1979.

Donath's Hierarchical Placement Model

3. Each subcircuit (module) is mapped to a subgrid.



4. Repeat recursively until all logic blocks are assigned to exactly one grid cell in the Manhattan grid.

Donath's Length Estimation Model

At each level: Rent's rule gives number of connections

- number of terminals per module directly from Rent's rule (partitioning based Rent exponent *p*');
- number of nets cut at level *k* (N_k) equals

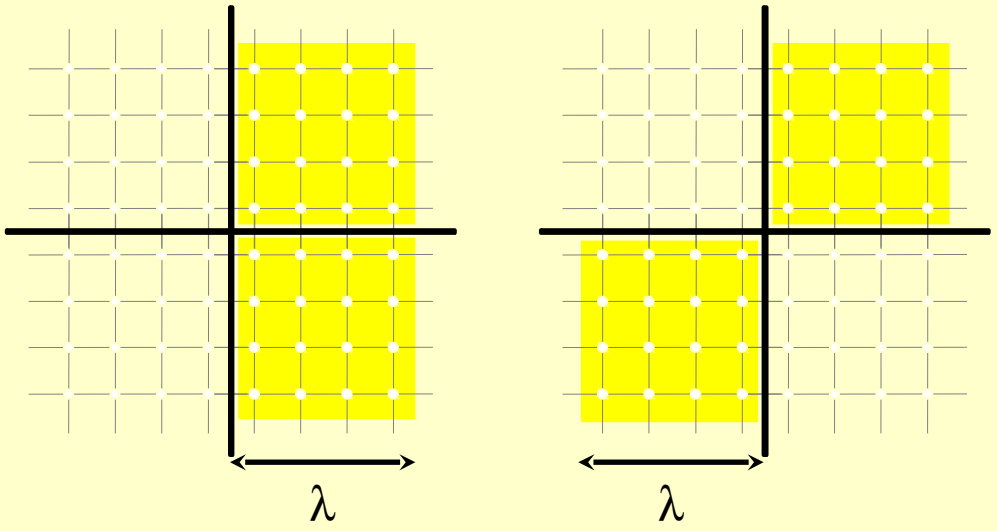
$$N_k = \alpha T_k$$

where α depends on the total number of nets in the circuit and is bounded by 0.5 and 1.

Donath's Length Estimation Model

Length of the connections at level *k* ?

Adjacent (A-) combination



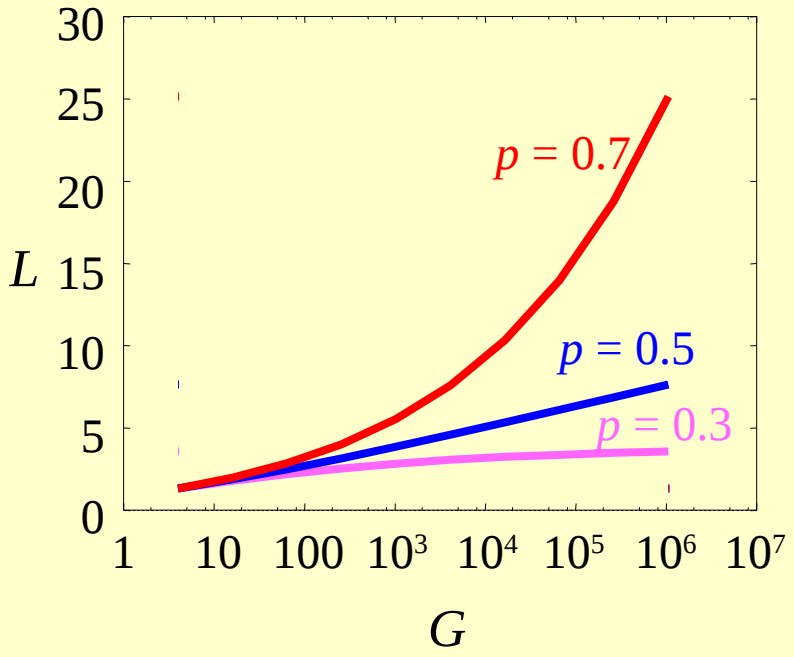
Diagonal (D-) combination

Donath assumes: all connection source and destination cells are uniformly distributed over the grid.

Results Donath

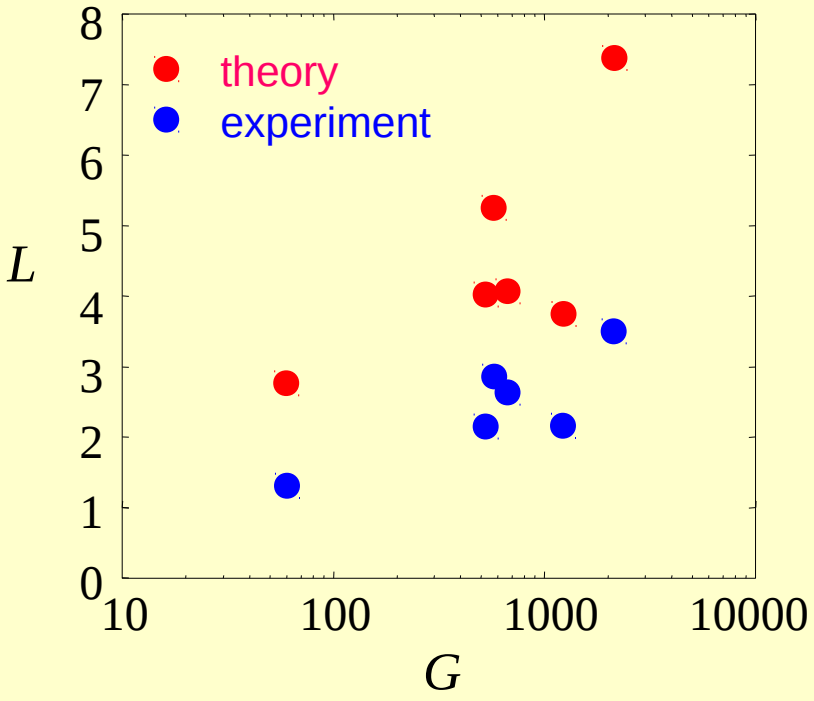
Scaling of the average length L as a function of the number of logic blocks G :

$$L \propto \begin{cases} G^{p-0.5} & (p > 0.5) \\ \log(G) & (p = 0.5) \\ f(p) & (p < 0.5) \end{cases}$$



Similar to measurements on placed designs.

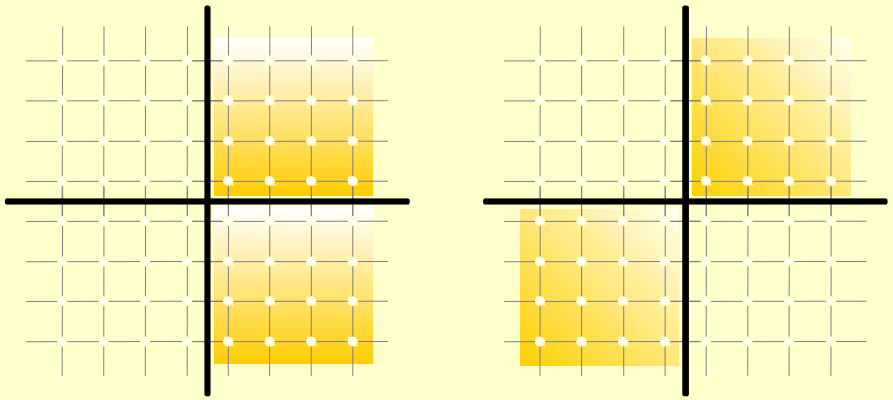
Results Donath



Theoretical average wire length too high by factor of 2

Improving on the Placement Optimization Model

- Keep wire length scaling by hierarchical placement.
- Improve on uniform probability for all connections at one level (not a good model for placement optimization).



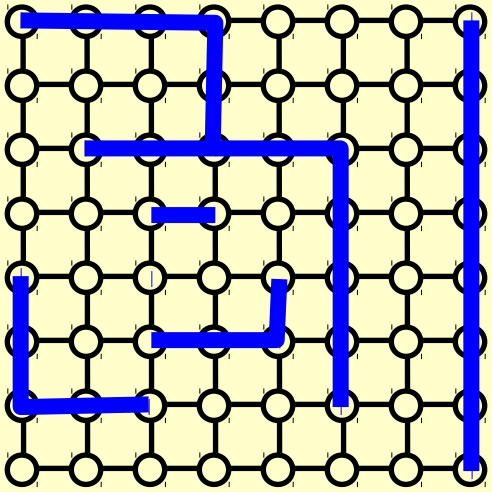
Occupation probability* favours short interconnections (for placement optimization) (darker)

* D. Stroobandt and J. Van Campenhout. Accurate Interconnection Length Estimations for Predictions Early in the Design Cycle. *VLSI Design, Spec. Iss. on PD in DSM*, 10 (1): 1-20, 1999.

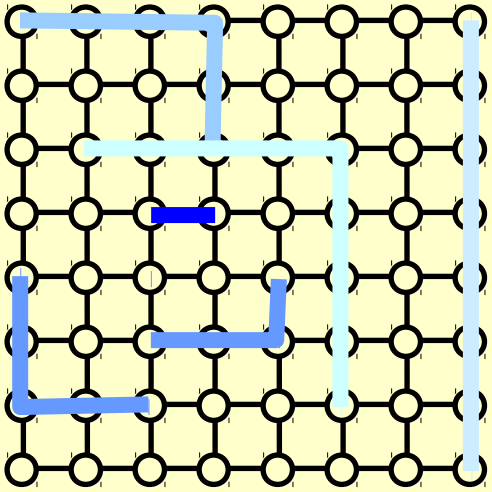
Including Placement Optimization

Wirelength distributions contain two parts:

site density function and probability distribution



all possibilities
requires enumeration
(use generating polynomials*)

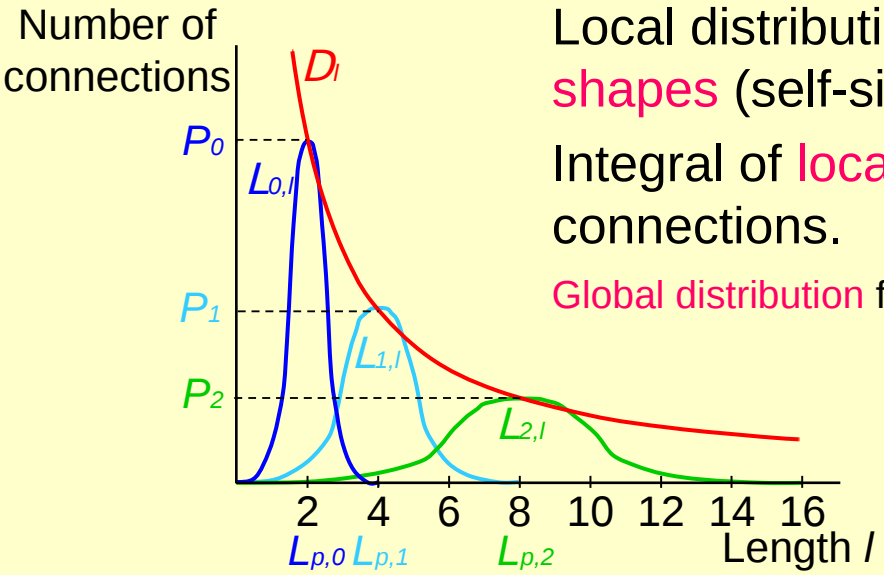


probability of occurrence
shorter wires more probable

$$N(l) = K\, D(l)\, q(l)$$

* D. Stroobandt and H. Van Marck. “Efficient Representation of Interconnection Length Distributions Using Generating Polynomials.” *Workshop SLIP 2000*, pp. 99-105, 2000.

Occupation Probability Function



Local distributions at each level have similar shapes (self-similarity) ⇒ peak values scale.

Integral of local distributions equals number of connections.

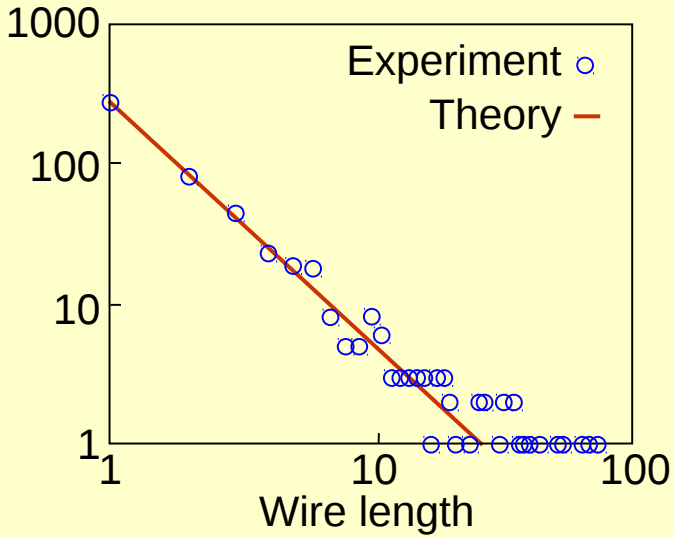
Global distribution follows peaks.

From this we can deduct that

$$N(l) \propto l^{2p-3}$$

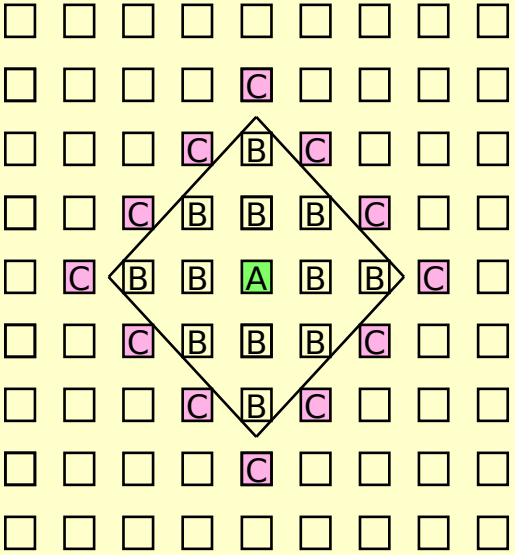
For short lengths: $D(l) \propto l$

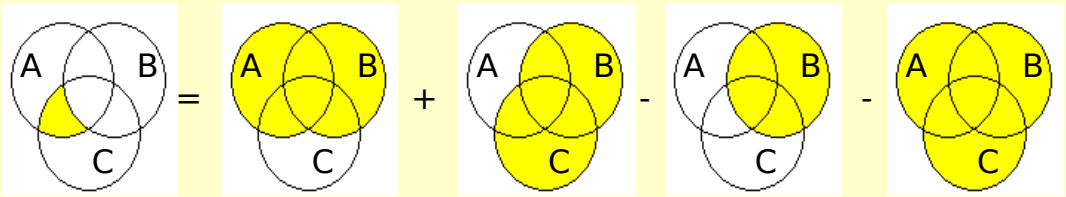
$$\Rightarrow q(l) \propto \frac{N(l)}{D(l)} \propto l^{2p-4}$$



Occupation Probability Function

Same result found by using a terminal conservation technique*





$$T_{A\to C} = T_{AB} + T_{BC} - T_B - T_{ABC}$$

Assumption: net cannot connect A,B, and C

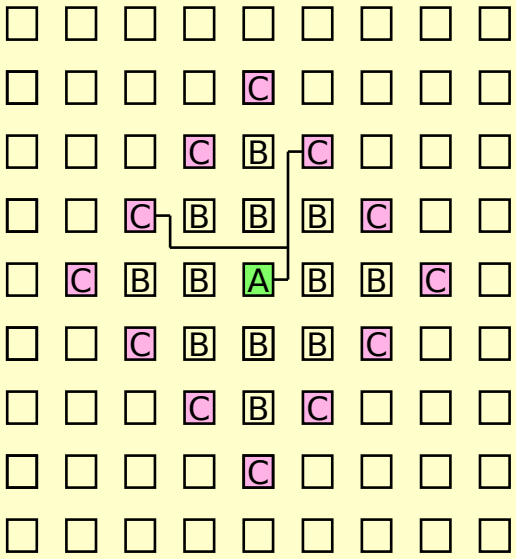
$$T_{AB} = t\left(1+B_B\right)^p \qquad T_{BC} = t\left(B_B+B_C\right)^p$$

$$T_B = tB_B^{\,p} \qquad T_{ABC} = t\left(1+B_B+B_C\right)^p$$

$$N_{A\to C} = \alpha T_{A\to C} = \alpha t\left[\left(1+B_B\right)^p + \left(B_B+B_C\right)^p - B_B^p - \left(1+B_B+B_C\right)^p\right]$$

* J. A. Davis et al. A Stochastic Wire-length Distribution for Gigascale Integration (GSI) - PART I: Derivation and Validation. *IEEE Trans. on Electron Dev.*, 45 (3), pp. 580 - 589, 1998.

Occupation Probability Function



For cells placed in infinite 2D plane

$$B_C = 4l$$

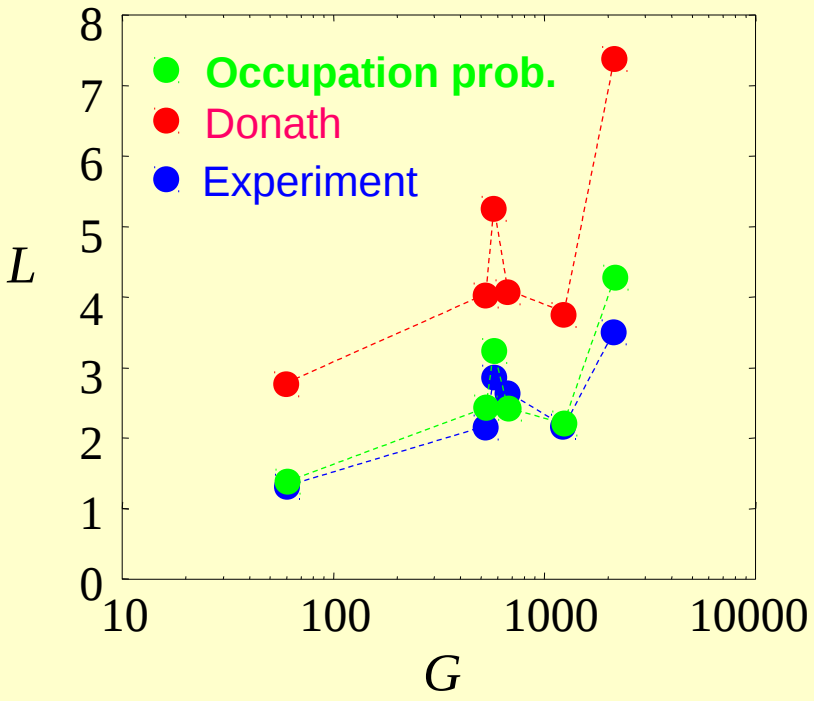
$$B_B = \sum_{l'=1}^{l-1} 4l' = 2l(l-1)$$

$$N_{A\to C} = \alpha t\left[\left(1+2l(l-1)\right)^p + \left(2l(l-1)+4l\right)^p - \left(2l(l-1)\right)^p - \left(1+2l(l-1)+4l\right)^p\right]$$

$$q(l) = \frac{N_{A\to C}}{4l} \propto l^{2p-4}$$

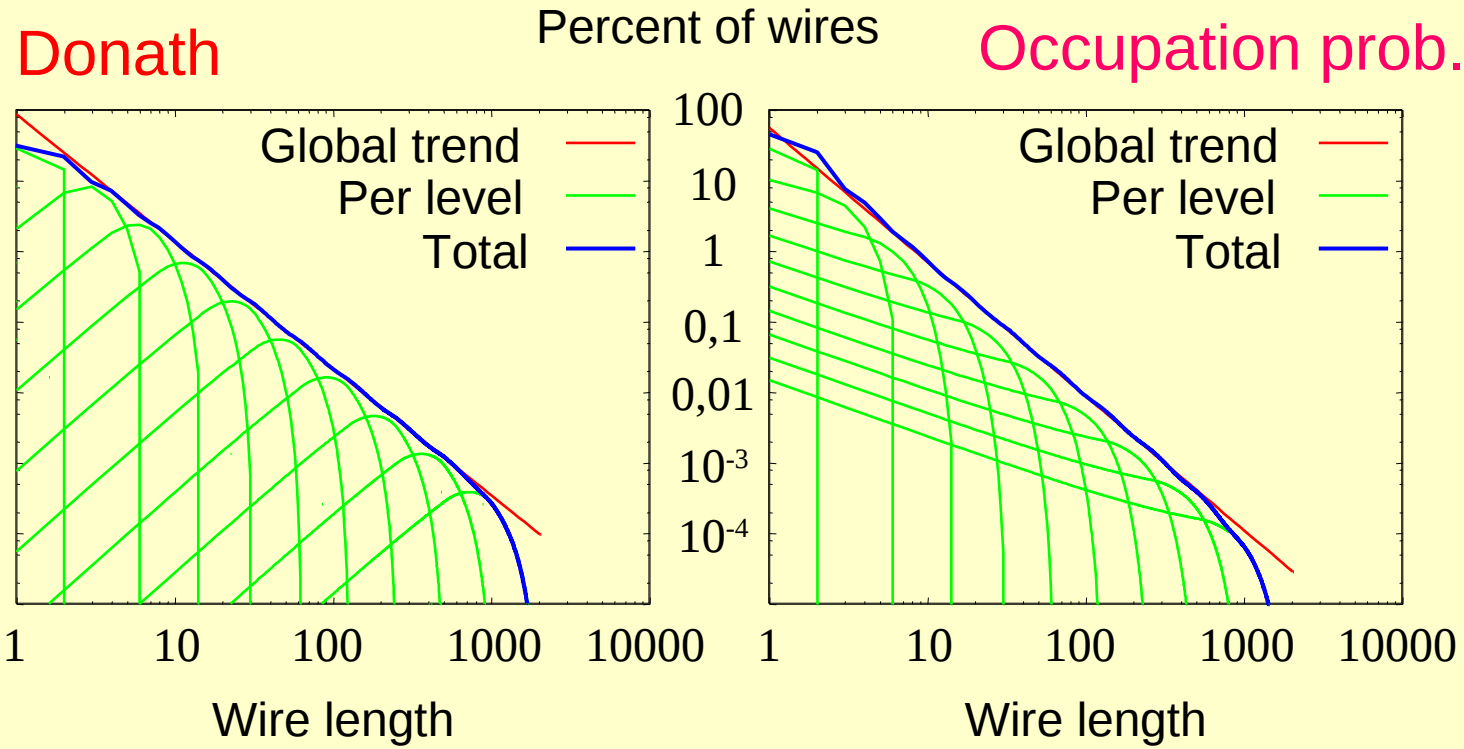
Occupation Probability: Results

Use probability on each hierarchical level (local distributions).



Occupation Probability: Results

Effect of the occupation probability: boosting the local wire length distributions (per level) for short wire lengths

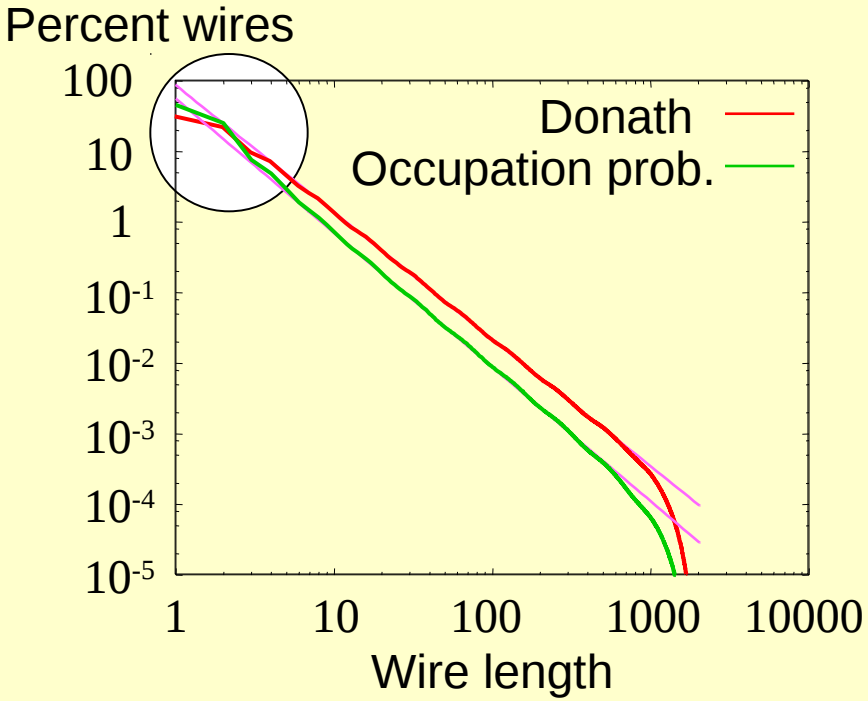


Occupation Probability: Results

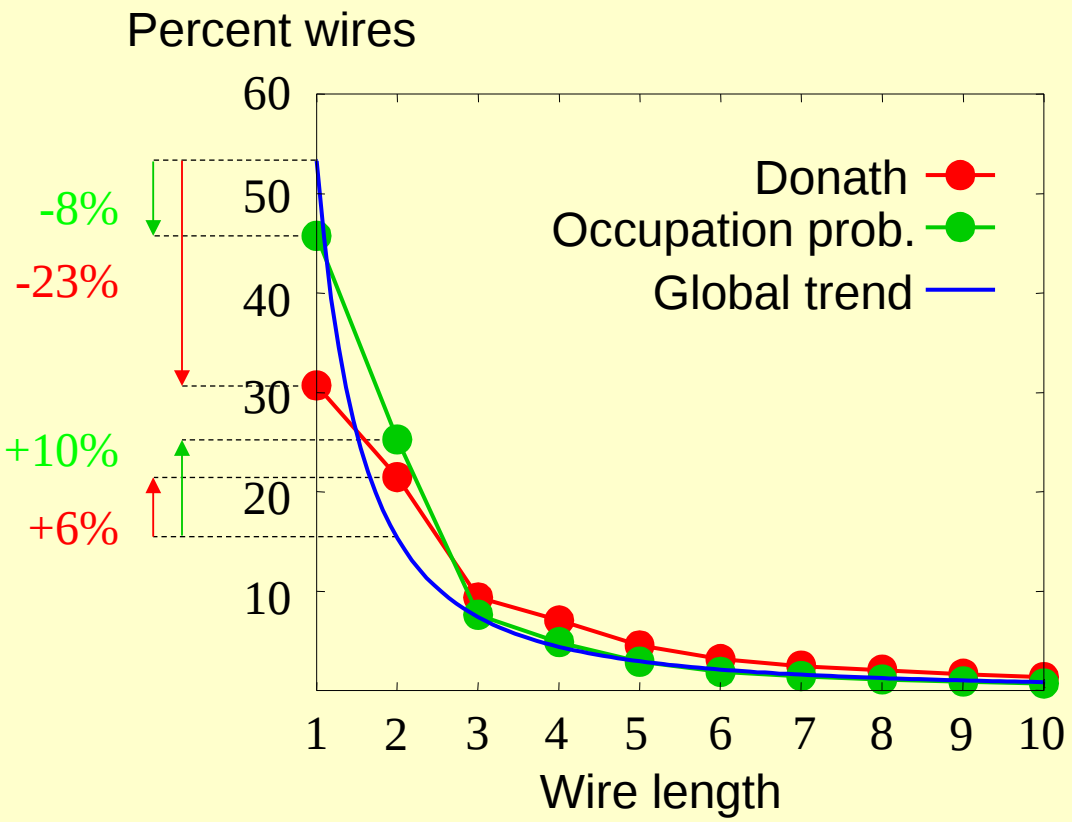
Effect of the occupation probability on the total distribution: more short wires = less long wires

⇓

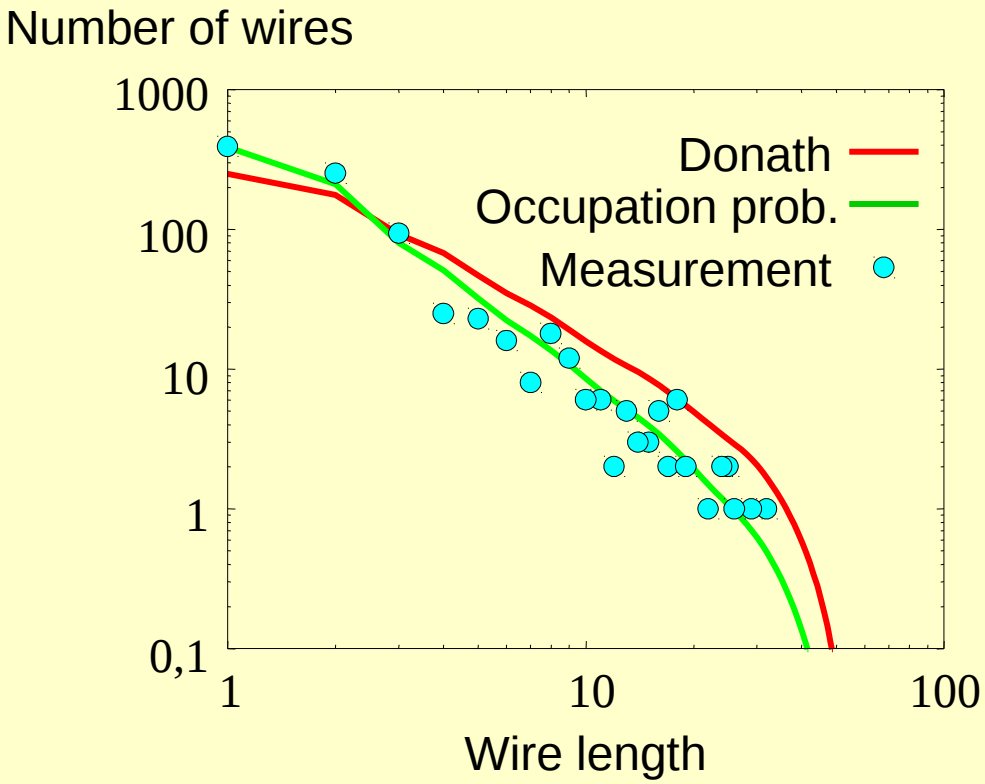
Average wire length is shorter



Occupation Probability: Results



Occupation Probability: Results



Outline

Why a priori interconnect prediction?

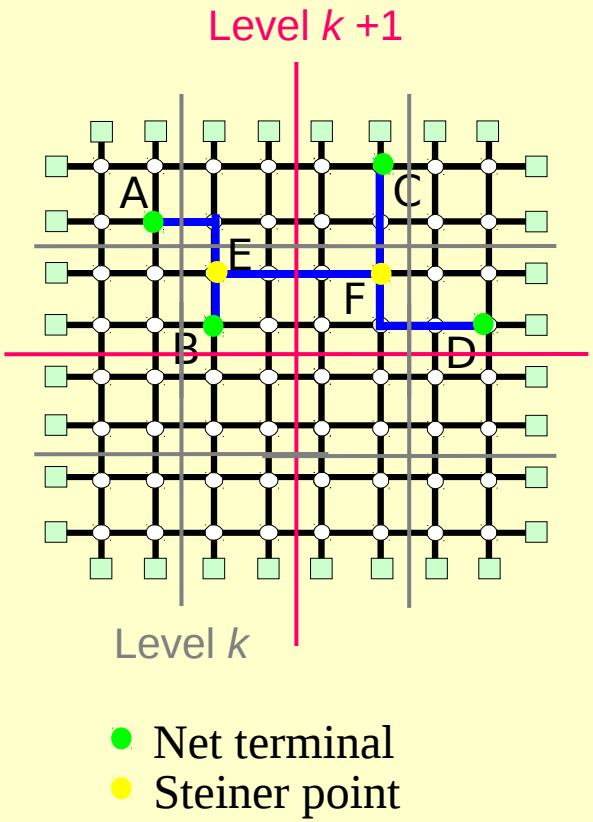
Basic models

Rent's rule

A priori wire length prediction

Recent advances

Length of Multi-terminal Nets



Difference between delay-related and routing-related applications*:

- Source-sink pairs

  Assume A is source

  A-B at level *k*

  A-C and A-D at level *k*+1

  Count as three connections

- Entire Steiner tree lengths

  Segments A-B, C-D and E-F

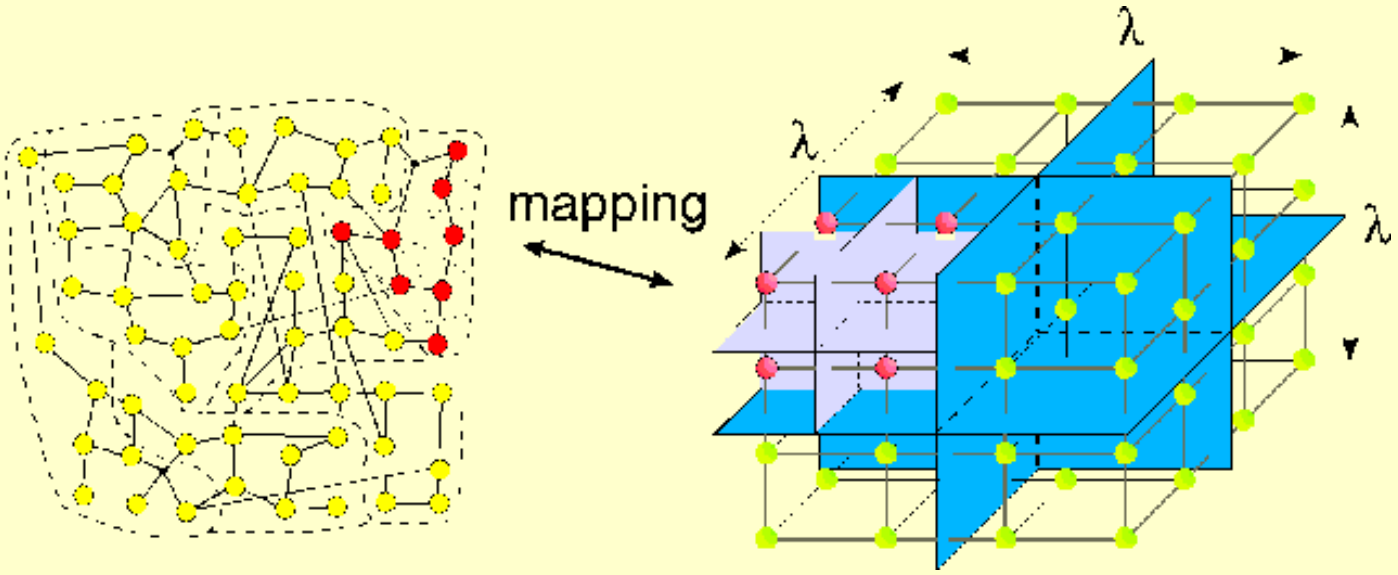
  A-B and C-D at level k

  E-F at level *k*+1

  Add lengths to one net length

* D. Stroobandt. “Multi-terminal Nets Do Change Conventional Wire Length Distribution Models.” *Workshop SLIP 2001*.

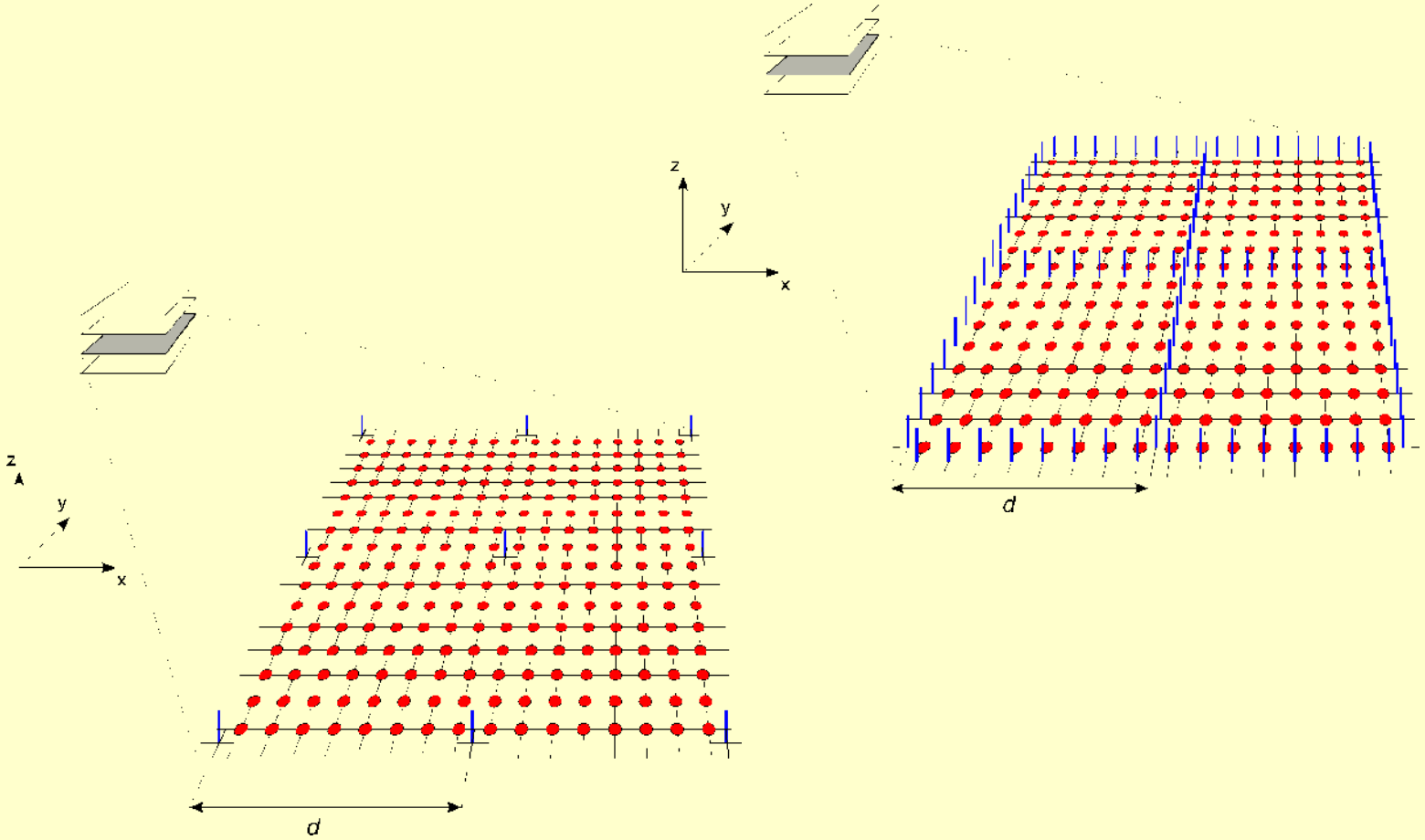
Extension to Three-dimensional Grids*



* D. Stroobandt and J. Van Campenhout. “Estimating Interconnection Lengths in Three-dimensional Computer Systems.” *IEICE Trans. Inf. & Syst., Spec. Iss. On Synthesis and Verification of Hardware Design*, vol. E80-D (no. 10), pp. 1024-1031, 1997.

* A. Rahman, A. Fan and R. Reif. “System-level Performance Evaluation of 3-dimensional Integrated Circuits.” *IEEE Trans. on VLSI Systems, Spec. Iss. on SLIP*, pp. 671-678, 2000.

Anisotropic Systems*



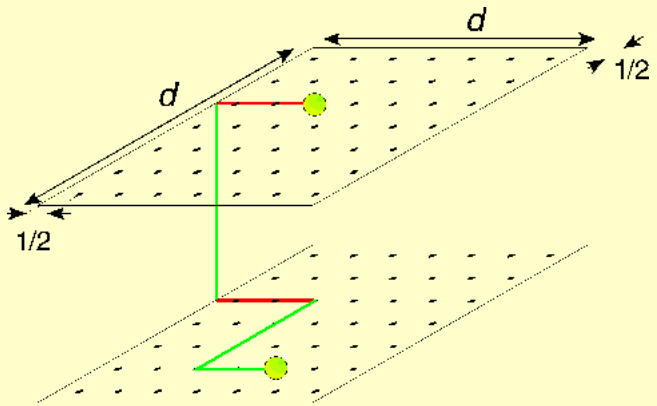
* H. Van Marck and J. Van Campenhout. Modeling and Evaluating Optoelectronic Architectures. *Optoelectronics II*, vol. 2153 of SPIE Proc. Series, pp. 307-314, 1994.

Anisotropic Systems

Not all dimensions are equal (e.g., optical links in 3rd D)

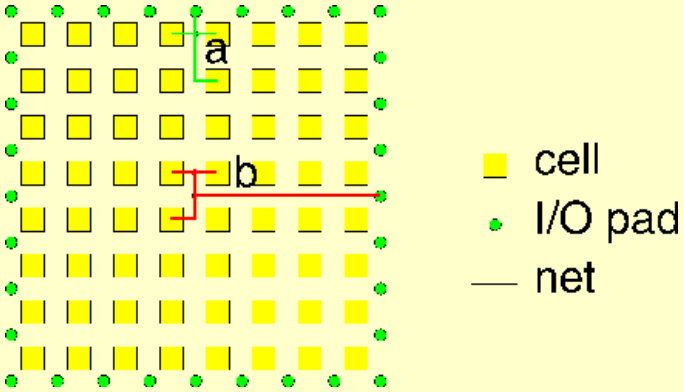
- Possibly larger latency of the optical link (compared to intra-chip connection);
- Influence of the spacing of the optical links across the area (detours may have to be made);
- Limitation of number of optical layers

Introducing an optical cost



External Nets

Importance of good wire length estimates for external nets* during the placement process:

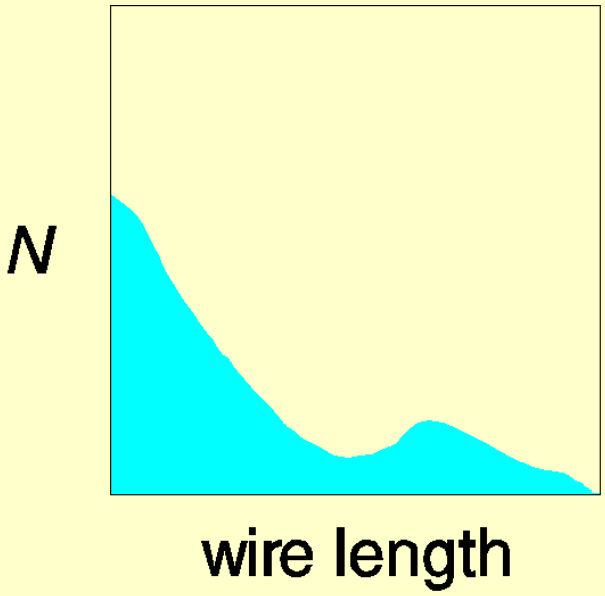


For highly pin-limited designs: placement will be in a ring-shaped fashion (along the border of the chip).

* D. Stroobandt, H. Van Marck and J. Van Campenhout. Estimating Logic Cell to I/O Pad Lengths in Computer Systems. *Proc. SASIMI'97*, pp. 192-198, 1997.

Wire Lengths at System Level

At system level: many long wires (peak in distribution).



How to model these?

Estimation* based on Rent's rule with the floorplanning blocks as logic blocks.

* P. Zarkesh-Ha, J. A. Davis and J. D. Meindl. Prediction of Net length distribution for Global Interconnects in a Heterogeneous System-on-a-chip. *IEEE Trans. on VLSI Systems, Spec. Iss. on SLIP*, pp. 649-659, 2000.

Conclusion

Wire length distribution estimations have evolved a lot in the last few years and have gained accuracy but the work is not finished!

Suggested reading (brand new book):

D. Stroobandt.
A Priori Wire Length Estimates for Digital Design.
Kluwer Academic Publishers,
2001. 324 pages,
ISBN no. 0 7923 7360 x.