The TAXI transmission card and Fairisle/Yes/Maybe Protocol Xilinx Chip

Mark Hayter

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The Fairisle port controllers have a daughter board which contains the transmission system. The interface to the port controller is based around fifos to perform speed matching between the port controller and the network. A design has been done for a Xilinx 3020 programmable gate array for interfacing between the port controller and a TAXIchip driven line running the Fairisle/Yes/Maybe protocol. The version 3 port controllers (FPC3) have the transmission system on the main PCB, and have a revized control xilinx on a larger 3030 chip. The differences of the FPC3 version are described in the FPC3 Xilinx design document.

The organisation of the transmission card is shown in figure 1.

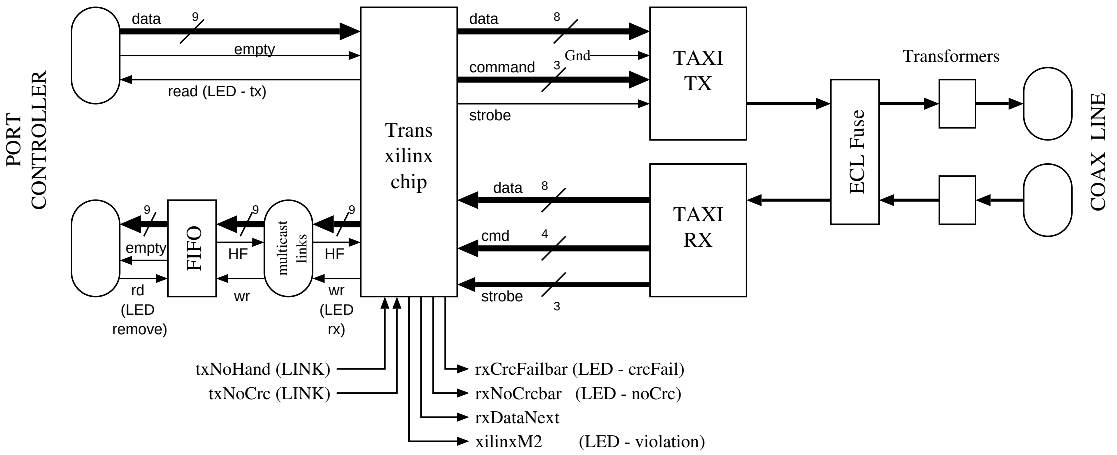

Figure 1: Fairisle TAXI Transmission Card

1 The transmission card Xilinx chip

The transmission card xilinx chip performs three main tasks. It controls the transfer of data between the TAXIchips on the transmission line and the FIFOs to the port controller. Also it can insert the CCITT header error check CRC to cells being transmitted and check and remove the CRC from received cells. The final task is to control hardware handshaking over the transmission line using a simple Xon/Xoff protocol.

Table 1 gives details of the pins on the xilinx chip. Most are used to control the fifos or TAXIchips. The other pins are discussed below.

Name	Direction	Use
Reset	In	Reset the chip
txClk	In	TAXI transmit clock
rxClk	In	TAXI receive clock
txFifoEbar	In	Empty signal from transmit fifo
txFifoRbar	Out	Read strobe to transmit fifo
txfD[0-8]	In	Data from transmit fifo
txNoCrc	In	CRC insertion disable
txNoHand	In	Handshake disable
txtD[0-7]	Out	Data to transmit TAXIchip
txtC[0-2]	Out	Command to transmit TAXIchip
txtStrobe	Out	Strobe transmit TAXIchip
rxtVltn	In	Violation signal from receive TAXIchip
rxtDstrb	In	Data strobe from receive TAXIchip
rxtCstrb	In	Command strobe from receive TAXIchip
rxtD[0-7]	In	Data from receive TAXIchip
rxtC[0-3]	In	Command from receive TAXIchip
rxDataNext	Out	Set on falling rxClk to indicate data at rising rxClk
rxfD[0-8]	Out	Data to receive Fifo
rxFifoWbar	Out	Write strobe to receive fifo
rxFifoHFbar	In	Half full signal from receive fifo
rxCrcFailbar	Out	Low if a cell fails its CRC
rxNoCrcbar	Out	Low if current cell has no CRC
xilinxM2	In/Out	Configuration input then violation indicator

Table 1: Pins on trans chip

To ensure correct behaviour in the presence of disconnected or noisy transmission lines the xilinx chip will detect the "violation" signal from the receiving TAXIchip and stop accepting data. The line has to be clear from violations for 64 character times before data will again be accepted. While seeing violations, or in the recovery period an indication is put out on the "xilinxM2" line.

1.1 Special pins

This section discusses the special pins on the trans chip. Note that commands and cell formats are as in the proposed Fairisle/Yes/Maybe protocol. Both the Soc and Sno cell formats are supported, and the transmission format may be changed from cell to cell[1].

- **txNoCrc**. This pin is used to enable or disable the insertion of the CRC into the transmitted data stream. If this pin is low then a cell will be started with a Soc command and the CCITT CRC of the first four (ie header) bytes will be inserted as the fifth in the cell. If the pin is high then the Sno command is used to start the cell and no CRC is inserted. The state of this pin should only be changed between cells, if it is

[1] Though I can't see why you would want to!

altered during transmission of a cell then the cell being transmitted may be corrupted[2].

- **txNoHand**. This pin is used to enable or disable the Xon/Xoff handshaking. If this pin is set then the chip will never generate or respond to Xoff. It will always send Xon as a response to a Held command from the other end.

- **rxDataNext**. This pin is used to indicate valid data on the rxfD[0-7] lines. It is intended for use when the trans chip is not being used to drive a fifo directly[3]. The output changes on the falling edge on rxClk to indicate the validity of data after the next rising edge. If rxDataNext is high after falling rxClk then there will be valid data placed on the lines after the next rising edge, otherwise the data is undefined.

- **rxCrcFailbar**. This pin will go low if the received cell contains a CRC and the CRC does not match that in the cell. The first few bytes of the cell will have been presented on the output lines, but no further bytes will be output until the start of cell for the next cell. It is expected that the receiving system will be able to deal with such short cells.

- **rxNoCrcbar**. This pin will go low if a cell is received containing no CRC (ie one which starts with an Sno command) and go high if a cell containing a CRC (ie starting with Soc) is received.

- **xilinxM2**. This pin has two uses. Until the xilinx chip has been configured (or during reconfiguration) it is the M2 input line, which indicates the programming method. For serial master mode programming the line should be pulled low through a resistor. Once configured the line becomes an output and indicates a violation on the reception line, or the recovery period following a violation. The output is driven low to indicate the violation state. On the Fairisle card this signal is required for the driver of the "violation" LED[4].

1.2 Handshake

The hardware handshake is done on a per cell basis. If the receive fifo is over half full when a start of cell command is received, and handshaking is enabled, then an Xoff command will be sent. An Xon command will be sent when the fifo falls below half full following transmission of an Xoff, or if a Held command is received and the fifo is less than half full.

If enabled in response to an Xoff the transmission system will stop just before sending a start of cell command. It will then send the Held command every 8th character time, with Sync commands in between, until Xon is received.

The handshaking is of no use over long links (where many cells are stored in the transmission medium) and is of doubtful value between switches. However it may be of use on direct links between hosts, and on host-switch links.

[2] At the moment I think there would be no problems but Im not going to any effort to ensure this remains so

[3] eg when the multi-cast node is in use

[4] Thus on the Fairisle card a violation will be spuriously signalled by an unprogrammed or reprogramming xilinx chip.

Colour	Name	Indicates
Red	Violation	A line violation is being seen, or the xilinx is unprogrammed or in reset.
Red	Bad CRC	A cell containing a HEC CRC was received but rejected because the CRC was wrong.
Red	No CRC	A cell not containing a HEC CRC was received.
Red	Mcast	Available for the multi-cast node to use.
Green	Insert	Bytes are being inserted in the receive FIFO.
Green	Remove	Bytes are being removed from the receive FIFO.
Green	Transmit	Bytes are being transmitted.
Green	Power	The card is powered.

Table 2: LEDs on the card (top to bottom)

1.3 Notes

The transmission TAXIchip command line c[3] is not driven by the xilinx, and should be tied low. This limits the xilinx to generating commands 0-7, but most of the others should be avoided anyway.

2 Slow transmission

There is a version of the xilinx bits which has the transmission side of the system slowed. This is done by forcing the insertion of sync marks in the data stream, and only enabling transmission one byte time in **n**. The value of **n** is fixed by the xilinx, and to change it the lca has to be modified and the bits regenerated. This will allow experiments to be done with slow transmission lines without modification to the hardaware. The txrx chip on the FPC3 (described along with the main FPC3 xilinx chip) allows the slow speed to be changed under software control.

3 Links on the TAXI transmission card

The transmission card has two links to control insertion of CRCs and handshaking commands. The "HANDLK" should be set to "1" to disable the use of handshaking, and to "0" to enable it. The "CRCLK" should be set to "1" to disable transmission of header CRCs and to "0" to enable. In addition the transformers joining the card to the coax line may be placed in the North end of their sockets to put the ECL I/O on the pins linking to the motherboard, or to the South end of their sockets to send the ECL I/O to the COAX connectors on the card itself. Links "L0" to "L7" should be made if no multi-cast card is in use, and together with the "P" and "M" points provide the socket for the multi-cast node to plug in.

4 LEDs on the transmission card

The transmission card as eight status LEDs, four red and four green. Table 2 lists their use. The green LEDs are usually on for too short a time to be seen.

5 Patches to the issue 1 card

The issue 1 TAXI transmission card has four patches:

1. The FIFO pin 7 () should be linked to FIFO pin 14 (GND).
2. The FIFO pin 23 () should be linked to FIFO pin 28 (+5).
3. The Transmit TAXI chip 12 should have the plated through hole drilled out and insulated, the socket pin being connected to the track from the xilinx to the transmission TAXI pin 15.
4. The track from the xilinx to transmission TAXI pin 15 should be cut, and the pin linked to GND. This is located on the capacitor pin south-east of pin 15 looking at the underside of the board. (Capacitor DCXIL1 pin 2).