ATM DOCUMENT COLLECTION 3
(The *Blue* Book)

March 1994

Preface to the Third Collection

This report contains the current versions of the documents associated with the ATM networking projects, including the Desk Area Network, at the University of Cambridge Computer Laboratory. These are intended mainly for reference by people involved with the projects on a day to day basis, rather than as a general overview. The hardware, software and protocols described in these documents are all under active development, so the details will change.

As a new departure, this year sees the inclusion of a number of papers in various stages, from submitted through to already presented, associated with or derived from the ATM work.

Various laboratory technical reports and Ph.D dissertations also include additional information over and above that present here. The MultiService Network Architecture is presented in Derek McAuley's thesis (technical report 186). Background to the Fairisle project may be found in the paper by Ian Leslie and Derek McAuley presented at SIGCOMM'91 (Proc SIGCOMM'91 page 327, also included in technical report 219). Joe Dixon's Ph.D thesis (technical report 245) contains a description of the networking software used and the Wanda micro-kernel. Some other ideas are presented in the "ATM Everywhere" article in IEEE Network magazine.

The initial paper on the Desk Area Network may be found in the paper by Mark Hayter and Derek McAuley in Operating Systems Reviews, Vol 25 No 4, October 1991, (also technical report 228). Also Mark Hayter's thesis is now available as technical report 319 and provides a good overview of the current Cambridge ATM environment, including the current status of the DAN.

This document can be retrieved in postscript form from the machine `ftp.cl.cam.ac.uk` in directory `/public/reports/ATM/docs-94-3`, and is available on the World Wide Web via `http://www.cl.cam.ac.uk/`. To save on trans-atlantic bandwidth it can also be retrieved from `cell-relay.indiana.edu` in directory `/pub/cell-relay/docs/ftp.cl.cam.ac.uk/94-3`. Postscript versions of recent technical reports can also be found on `ftp.cl.cam.ac.uk` in directory `/public/reports`. Paper copies of technical reports can be ordered by sending mail to `tech-reports@cl.cam.ac.uk`.

This document is intended to replace the earlier first and second ATM Collections (the "Yellow" and "Orange" books). Of the documents in the second collection some thirteen are no longer included. This is mostly because the equipment or protocols they described have been superseded. Although there is not currently any formal collaboration with Olivetti Research Ltd on ATM, some documents describing hardware designed by them remain in the collection because it is still in active use within the Computer Laboratory.

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ATM Protocols

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Glossary of Terms

AAL	ATM Adaptation Layer
ACK	Acknowledge
ADC	Analogue Digital Convertor
ALO	At Least Once (RPC semantics)
AMO	At Most Once (RPC semantics)
ANSA	Advanced Networked Systems Architecture
ARM	Advanced RISC Machine
ASIC	Application Specific Integrated Circuit
ATM	Asynchronous Transfer Mode
AUU	ATM User User indication, "the bit", end of AAL5 block marker
AVA	ATM Video Adaptor
BARF	Broken
B-ISDN	Broadband Integrated Services Digital Network
BT	British Telecom
CAC	Connection Admission Control
CBN	Cambridge Backbone Network
CBR	Constant Bit Rate
CCD	Charge Coupled Detector (part of a camera)
CCITT	Comitée Consultatif International Télégraphique et Téléphonique (now the ITU-TS)
CLP	Cell Loss Priority (a bit in a B-ISDN cell header)
CRC	Cyclical Redundancy Check
CUCL	University of Cambridge Computer Laboratory
DAC	Digital to Analogue Convertor
DAN	Desk Area Network
DCT	Discrete Cosine Transform (used in video compression)
DFS	DAN Frame Store
DMA	Direct Memory Access
DPL	Distributed Programming Language (part of ANSA)
DRAM	Dynamic RAM
DSP	Digital Signal Processor
E1	2 Mbit/sec
E2	8 Mbit/sec
E3	34 Mbit/sec

EATM	EISA ATM (an adaptor)
ECL	Emitter Coupled Logic
EDL	Ethernet Data Link
EISA	Enhanced Industry Standard Architecture (a bus)
ESIC	EISA control ASIC
EXO	Exactly Once (RPC semantics)
FDDI	Fiber Distributed Data Interface
FAS	Framing and Sequencing
FDL	Forty-eight Data Link
FIFO	First In First Out
FIQ	Fast Interrupt Request (on ARM processors)
FPC	Fairisle Port Controller
FPC1	Fairisle Port Controller Revision 1
FPC2	Fairisle Port Controller Revision 2
FPC3	Fairisle Port Controller Revision 3
FPGA	Field Programmable Gate Array
FRC	Free Running Clock
GFC	Generic Flow Control (a 4 bit field in a B-ISDN cell header)
H.261	A constant bit rate video compression standard.
HEC	Header Error Check (an 8 bit CRC in a B-ISDN cell)
IDL	Interface Definition Language (part of ANSA)
IOB	Input Output Block (on a Xilinx FPGA)
IOC	Input Output Controller
IP	Internet Protocol
IPA	India Pale Ale
IRQ	Interrupt Request
ISDN	Integrated Services Digital Network
ISO	International Standards Organisation
ITU	International Telecommunication Union
JSAC	Journal Select Area Communications ("jay sack")
JPEG	Joint Photographic Experts Group (a video compression standard)
LAN	Local Area Network
LCA	Logic Cell Array
LRU	Least Recently Used
MAC	Media Access Control

MAN	Metropolitan Area Network
MDH9	The DAN CPU Node
MDL	Media Data Link
MEMC	Memory Controller
MIDDL	Mothy's Interface Definition Language
MMU	Memory Management Unit
MPEG	Motion Picture Experts Group (a video compression standard)
MPS	Message Passing Service (part of ANSA)
MSDL	MultiService Data Link
MSDR	MultiService Data Representation (the wire data format for MSRPC)
MSNL	MultiService Network Layer
MSNA	MultiService Network Architecture
MSRPC	MultiService RPC
MSRPC2	MultiService RPC Version 2
NACK	Negative Acknowledgement
NOSSDAV	Network and Operating System Support for Digital Audio and Video ("nose dive")
NETCON	Network Console
NNI	Network Network Interface
NPC	Null Port Controller
NRL	Nemesys Research Ltd.
OC3	155 Mbit/sec
OC12	622 Mbit/sec
ORL	Olivetti Research Limited (Cambridge)
OS	Operating System
OSI	Open Systems Interconnection
PAL	Programmable Array Logic
PCB	Printed Circuit Board
PDH	Plesiochronous Digital Hierarchy
PDU	Protocol Data Unit (a packet)
PIO	Programmed Input Output
PLT	Payload Type (a 3 bit field in a B-ISDN cell header)
PTM	Packet Transfer Mode
Q.93B	The Standard (i.e. awful) ATM signalling protocol
QOS	Quality of Service

RARP	Reverse Address Resolution Protocol
REX	Remote Execution Protocol (part of ANSA)
RGB	Red, Green, Blue (video decomposition)
RISC	Reduced Instruction Set Computer
RPC	Remote Procedure Call
SAM	Serial Access Memory
SAP	Service Access Point (a communications endpoint)
SAR	Segmentation and Reassembly
SAS	Single Address Space
SBUS	Sun Bus
SDH	Synchronous Digital Hierarchy
SDL	Standard Data Link
SDU	Service Data Unit (a packet)
SOC	Start of Cell
SONET	Synchronous Optical Network
SPROING	To Break
SRAM	Static RAM
SSCOP	Signalling System Common Operations Protocol (the standard (i.e. awful) transport protocol for carrying Q.93B)
STM	Synchronous Transfer Mode
STS1	155 Mbit/sec
STS4	622 Mbit/sec
T1	1.5 Mbit/sec
T3	45 Mbit/sec
TAXI	Transparent Asynchronous Transmitter/Receiver Interface
TBUF	Tristate Buffer (on a Xilinx FPGA)
TDM	Time Division Multiplexing
TPDRAM	Triple Ported DRAM
TLB	Translation Lookaside Buffer
UDL	Unison Data Link
UNI	User Network Interface
VC	Virtual Channel or Virtual Circuit
VCI	Virtual Circuit Identifier (also Virtual Channel Identifier)
VM	Virtual Memory
VP	Virtual Path

VPI	Virtual Path Identifier
VRAM	Video RAM
WAN	Wide Area Network
WDBS	Wanda Dumb Boot Server
WDFS	Wanda Dumb File System
WJWP	Wanda Jumping Window Police
XDR	External Data Representation (the wire data format for SUN RPC)
Xi3	Xilinx revision 3
Xi5	Xilinx revision 5
Xi6	Xilinx revision 6
XTB	Xilinx Teaching Board
YCC	Luminance Chrominance Chrominance (video decomposition)
YUV	Luminance Chrominance Chrominance (video decomposition)