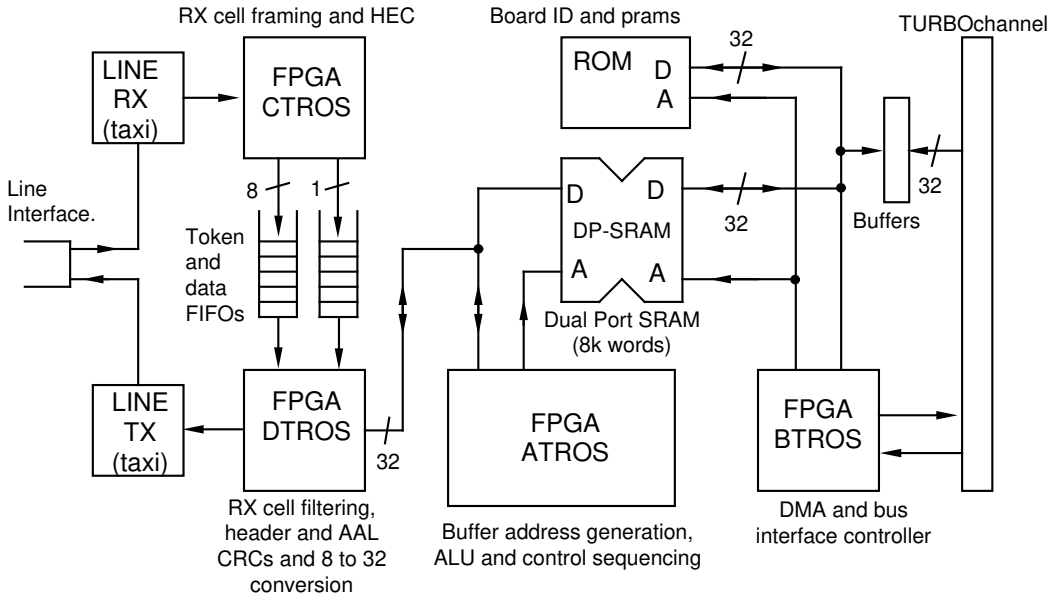

Figure 1: Block diagram of the 'Yes V3' option module.

- Double buffering using partitioning within slots. The memory allocation for each slot may be divided into two sub-slots to provide double buffering. This enables uninterrupted streaming on a given virtual circuit, by allowing the host to service one half of the slot while reception or transmission continues in the other half.
- Nine user registers including interface status register (ISR) and interface control register (ICR).
- A circular FIFO of completion events indicating work items completed by the interface and awating attention from the host processor. The host may either take an interrupt for each completion event, or just poll the head of the completion queue at appropriate times.
- When multiple outgoing VCs are busy, a scheduling mechanism is available to support fragmented transmit. This may either be round-robin or priority, according to whether the host links transmit slots into a ring or a queue.
- Rate control is available for any bandwidth-limited outgoing connections.
- Big or little-endian operation.
- Option ROM containing Turbochannel board identifier etc..

'YES V3-TC' A high performance ATM interface.

D J Greaves.

February 17, 1993

The 'Yes V3-TC' Turbochannel option module is a high performance ATM networking card available for systems which support the DEC Turbochannel option connector. The interface is designed to require a minimal host supervision thus freeing host CPU cycles. The 'Yes V3-TC' Turbochannel option module was developed by Olivetti Research within the Esprit OSI 95 project.

Figure 1 is a block diagram of the option module. It transmits and receives ATM cells over a full-duplex, bi-directional coax cable. The modulation technique is 4B5B/NRZI using the AMD TAXI parts.

The 'Yes V3-TC' option module provides direct transfer of cell payloads between host address space and the serial line interface by autonomous DMA.

Cell headers are generated and checked within the interface. The only significant onboard cell buffer is the receive FIFO, shown in figure 1, which holds cells awaiting receive DMA in reception order. The token FIFO contains one entry per received cell, indicating the number of cells in the data FIFO and whether each had a valid HEC and frame length. Multiple areas of host RAM may be associated with each virtual circuit for scatter and gather operations.

Programming is done using shared data structures held in the onboard dual-ported SRAM. This is mostly devoted to a number of fixed size regions, termed 'slots', which each contain the full control state for a single incoming or outgoing virtual circuit.

The option module supports the following features:

- A galvanically isolated 50 ohm coax line interface, including an equaliser and a hybrid to offer duplex operation on a single cable.
- A pair of AMD TAXI chips for 100 Mbit/second full duplex communication. (As an option, higher speed TAXI chips may be fitted since the line clock rate is decoupled from host bus rate.)
- Three LED indicators: transmit active, receive active and line disconnected (or violation).
- ATM cell framing using 4+1+48 bytes header, header check and payload.
- For the adaptation layer, 32-bit CRC generation and checking according to the AAL-5 standard. Separate, running CRC residues are held for each active virtual circuit. (The Cambridge SAR-1 adaptation layer is also fully supported for local backwards compatibility.)
- 8K words of dual-ported static RAM mapped into user option address space and to option on-board resources. This SRAM is always available for host random access.
- Up to 12 descriptors for each virtual circuit, held in the SRAM. Each descriptor consists of a pair (host address, length). The individual lengths do not need to be a multiple of 48 bytes, but their sum should be.