Milway 16 bit CFR Interface for Archimedes
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1 Programming Model

The interface has a simple programming model. Address lines A13 and A12 control the basic operation, with A11 modifying the operation. All operation to the CFR part of the interface are MODULE type cycles. The Podule Id PROM is accessed with the normal PODULE cycles at any speed.

The CFR A0 register select input is connected to podule bus address wire A6 giving a register spacing of 64 bytes.

1.1 Basic Operations

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A13/A12/A11      Function
 0 / 0 / x       Byte operations. One cycle of 375nS.
 0 / 1 / s       Word operations. Two cycles of 125nS.
 1 / 1 / 0       Disable operations. One cycle of 500 nS.
 1 / 1 / 1       Interrupt Control.

   A11           Function
    x            Don't Care
    s            0 Little Endian, 1 Big Endian.
```

These timings assume an 8 MHz bus clock. They should be scaled as appropriate. For changing the configuration of the timing circuitry see section 4

1.2 Status and Interrupt Control Information

Bit 0 of the interrupt control location is a write only control flag. When one, interrupts are enabled. Writing either a one or a zero to the location clears the current interrupt (stored in a flip-flop external to CFR chip).

All board status information, ie IRQ and FIQ, can be read from word Zero of the PODULE ID PROM. These are found in the required bits. An additional bit of information is found in bit 8, (N.B. not bit 7) if this bit is a one then the board is connected to the network.

Reading this podule ID location also clears the interrupt flip-flop.

1.3 Podule Indentificantion

The podule rom contains a country code of zero (uk), a manufacturer code of two (olivetti) and a product code of zero (which seems a bit dubious).

2 Board Configuration

There are 3 configuration links which may be adjusted for normal operation.

Link 6 alows the selection of either IRQ or FIQ interrupts.

Link 3 is used in conjunction with the Map RAM. If the Map RAM is in place then link 3 should be removed. If the Map RAM is removed then link 3 should be inserted. With the Map RAM removed and link 3 inserted this disables the automatic rejection of packets.

Link 4 Selects normal station operation or bridge operation. If inserted the interface will operate in Bridge mode and if removed it will operate in normal station mode. There is no possibility of software selection. Note that reading the station address is unreliable in bridge mode and is therefore even less reliable than usual on this hardware if link 4 is selected.

The station address is stored in a PAL and may be read through the CMOS chip in the usual manner.

3 Board Status Information

There are 6 LEDs on the front panel of the board giving status information. These are numbered in the range 1 to 6 but not in order. They are, in order starting at the end with the network connector:

3 Indicates that the network is connected. (green)

2 Indicates if the PLL is in lock, and should always be on. (green)

1 Indicates if the are any modulation errors being detected and thus should be off. (red)

4 Indicates if there are any transmissions occuring.(yellow)

5 Indicates if there are any receptions occuring.(orange)

6 Indicates if there are any TOGS occuring.(red)

4 Board Setup

There are 3 SMB connectors and 1 link on the board for use in setting up the clock recovery circuit. Link 2 on the board is used to disable the phase signal, thus enabling the vco to be aligned with out the network being connected. Correct alignment can only be completed when the network is connected as the built in reference is not very accurate.

Connector J4 is a buffered version of the VCO output and must be terminated with a 50 Ohm impedance. J3 is a buffered version of the Phase Compare signal and must also be terminated with 50 Ohms. J1 is serial data output.

The VCO adjustment is made through L3, with large changes made by replacing C303 and C307 which are in parallel.

The Bus interface timing is controlled by Links 6, 7 and 8. Link 7 provides a set of timings which are selected by links 6 and 8. Link 6 should always be made towards pin 1 of link 7 and Link 8 away. **The connections should never cross over.** The links should never be changed unless you know what you are doing.