Command	Function
T	Enter terminal type.
I	Initialize
V	Redraw terminal display (v for review ?).
R	Reframe ring (only works at monitor).
Mc	Master enable. c=1,0,A on, off or automatic.
F	Enter write frame mode constantly.
S	Enter clear ring mode. Syns only outgoing.
1	Enter regular write frame (like F but with delay between each frame)

Table 8: Commands accepted by the Telemetry console display. User commands are listed in the top section.

to which one can type a command. The commands are

- 'R n' reset telemetry unit number n.
- 'V n' reset VME bus (processor) at station n.
- 'S n' set own station serial number to n.
- 'M n' toggle monitor station willingness of station n.

References.

[1] 'The Cambridge backbone network.' DJ Greaves D Lioupis and A Hopper. IEEE Infocom 90, San Fransisco June 1990. Also in Proceedings European Fibre Optic Conference (EFOC / LAN 88) Amsterdam, June 1988.

Offset	Contents
0x0	Transmit queue 0, cell 255
0x20	Transmit queue 0, cell 254
0x40	Transmit queue 0, cell 253
...	... ...
0x1FE0	Transmit queue 0, cell 0
0x2000	Transmit queue 1, cell 255
0x4000	Transmit queue 2, cell 255
0x6000	Transmit queue 3, cell 255
0x8000	Receive queue, cell 255

Table 7: V1DMA queue layout for random host access. Note that the queues operate in reverse order.

10 Other information

10.1 Random access to the FIFO buffer area.

Random access to the station buffer area is available for memory and connector testing purposes. The buffer area use is shown in table 7. Note that the circular buffers are used in reverse order from the VME natural memory order. Within a cell area, only the first nine (out of sixteen) 32-bit words are used by the station. The first word of a cell sits at offset zero in the cell area.

10.2 False traffic generation.

The V1DMA slow board includes a front panel switch which causes extra ring traffic to be generated on channel one. When active, the last 256 cells transmitted on channel one are repeatedly repeated in their original sequence. All empty slots on channel one will be used in the absence of any other traffic through the station. The switch has three positions : offline, online (centre position) and false-traffic enabled. When the switch is in the offline position, the station is offline regardless of the ICR bit.

10.3 Interleaved host access for multi-threaded programs.

The receive side and transmit side contain completely separate state. Therefore it is possible to context switch between RX and TX queue access, mid-cell, without interference.

Invalid operation will result if software attempts to start writing a new cell to another channel when the old cell has not been completely written to the old channel.

11 Monitor and Telemetry Operation

A 9600 baud terminal may be connected to any station. The operations available from this terminal monitor are shown in Table 8.

The only commands usually required are 'T' to set the terminal type, 'V' to redraw the telemetry display after terminal connection and 'I' to initialise things. Pressing 'T' generates a menu of terminal types and a single-letter response is required.

Pressing 'I' yields the prompt

```
Initialise (R/V/S/M) ==>
```

8 Optical Fibre Type

The stations use the 1300 nm wavelength at a launch power of 100 microwatts. FC/PC fibre optic connectors are used. The maximum length of fibre between stations is specified as 20 kilometres, although only 17 kilometres have been tried. (The specification was 30 kilometers on the more expensive first generation stations.)

9 Station Initialisation and Test Procedure

In order to initialise a station to a well ordered state, the following procedure is recommended:

- Check station presence by reading and checking the hardwired bits in the ISR.
- Perform station RESET operation.
- Write ICR, turning off interrupts and setting station offline.
- Clear map, writing zero to every location.
- Perform RX synch and TX synch.
- Read 36 bytes from RX fifo. Then read cells from the RX fifo until the RX logged bit becomes clear. An integral multiple of 36 bytes should be read, with the logged bit checked after each cell (group of 36 bytes).
- Write the ICR register setting the station ONLINE and with appropriate interrupt vector base and interrupt mask values.

When first powed up, the following verifications tests can be performed by diagnostic software.

- **Own Channel Test:** check that all four own channels can be selected via the ICR and read back through the ISR.
- **VCI map test:** Take the station offline and perform a memory test of the VCI map. Any standard memory test routine, taking into account the 64K $\times 4$ nature of the memory, is suitable.
- **VME bus and buffer test:** Full insertion of the Fast Board into the VME bus can be checked by writing and then verifying test bit patterns into the fifo buffer store area. Any of the locations shown in table 7 can be used. For random access to the buffers, note that there is a 32 bit word on every two byte boundary (even address). Correct access is best obtained using two 16 bit cycles for each word transfered, with both cycles addressing the same di-byte address. The high 16 bits (D31-D16) are always transfered first, whether reading or writing. The implied hidden state, i.e. whether the access is to the high or low 16 bits is reset with the RESET soft command.

5.2 Interrupt code 10 - Not ready.

An interrupt with code and vector 10 is generated upon the ready to not-ready transition of the 'ready' bit in the ICR. This interrupt condition is cleared with reset command. Do not reenable interrupts until the ring becames ready. Re-enabling interrupts should be done by the ring watchdog routine (or other timer controlled routine), provided the ring has become ready.

6 VCI Map

	Host Data Bit D7 D6 D5 D4	Function
0	0 0 0 0	Reception disabled
8	1 0 0 0	receive but do not interrupt
9	1 0 0 1	receive and interrupt on sequence one
10	1 0 1 0	receive and interrupt on start bit
11	1 0 1 1	receive and interrupt on start or sequence one
12	1 1 0 0	receive and always interrupt

Table 6: VCI look-up map entry format.

Table 6 shows the VCI look-up bit-map bit assignment. The bit-map is 64K entries long and each entry is 4 bits wide. The map can be read and written over the VME bus whenever the ISR 'ready' bit is set. Cycles made when not ready will not DTACK and will result in a VME bus time-out (bus event). Each map entry appears on processor data lines 4 through 7, spaced on two byte boundaries. It is necessary to use D16 cycles for access to the map. The first entry in the map space is for VCI 0x00 0x00 and the last for VCI 0xFF 0xFF. This last VCI cannot be used for data since the monitor station uses it for ring reframe.

Bit 7 of a map entry enables reception of cells with that VCI. Since the V1DMA stations do not use the Backbone Ring response mechanism, there are no restrictions on multiple stations receiving the same cell, provided each has bit 7 of its map set.

Under MDL (SAR-1), the cell sequence number sits in byte 2 of the cell (bits 16 to 23 of the first 32 bit word). The start and prtfull bits are in bits 7 and 6 of the third byte (D31 and D30 of the first word) respectively.

The exact functions of these bits can be reprogramed with an alternative PAL, but note that bits 0 to 5 of the third byte are not available as inputs to this PAL.

7 Miscellaneous links.

On the Fast board, link 2 (A0) should be made and links 1 and 3 should be open.

On the Slow board, links 7 and 6 should be made and link 8 should be open. The other links control interrupt request level, bus request level and VME base address, and should be set as descrived earlier.

On the Telemetry board there is a link for the AGC circuit in the receiver module. This should be set 'North' to the top of the board, to enable AGC control loop.

Base Vector	Code
7 6 5 4 3 2	1 0

Table 4: Interrupt vector format

IC1	IC0	
0	0	Packet reception event.
0	1	End of world.
1	0	Not ready.
1	1	Cambridge wins boat race.

Table 5: Interrupt code assignment

4.3 TX and RX synchs and RESET command

Writing to the TX or RX synch location causes the associated side of the station to perform a synchronisation command. The value written is ignored. This simply means that, for the RX side, any cell partially read by the host is discarded, however it is at least necessary to read the second 32 bit word from the interface before RXsynch will cause a discard. For the TX side, any cell partially written to the interface is discarded. Complete cells stored in the station's queues are unaffected.

Writing to the RESET location performs station reset functions. The value written is ignored. All bits of ICR are cleared. This does not interrupt the operation of the ring or the telemetry sub-system; it only clears the interface.

5 Interrupts

The VME bus interrupt level is set using links and a PAL on the slow board. The default level is 4 when J9 is made. For other interrupt levels J5 is level 7, J3 is level 6, J4 is level 5, J9 is level 4, J6 is level 3, J7 is level 2, J8 is level 1. This is just Milway ! Also, IC10 needs reprogramming for a level other than 4.

5.1 Interrupt Code 00 - Packet arrival

An interrupt with code 00 is generated upon packet arrival, provided the appropriate code is present in the VCI map. Whether a packet generates an interrupt is determined by the map entry for its VCI (see section 6).

The interrupt flag is cleared by reading the first word (D16 or D32) from the receive fifo. This is so, regardless of the number of cells stored in the receive FIFO. It is necessary to poll the status register after each cell has been read to determine whether there are further cells buffered in the interface.

If there are no cells in the receive fifo when the packet arrival interrupt is issued, this means that a cell arrived at the station with a bad CRC and was discarded by the interface. It is an error to read the RX fifo when empty, so this type of interrupt must be explicitly detected by testing the ISR on interrupt routine entry and explicitly cleared with an RXSYNCH command.

Bit	Meaning
0	Rx fifo logged
1	Tx 0 logged
2	Tx 1 logged
3	Tx 2 logged
4	Tx 3 logged
5	
6	Interrupt type code IC0
7	Interrupt type code IC1
8	own channel bit 0
9	own channel bit 1
10	Online
11	Ready
12	always 1 (for board presence testing)
13	always 0
14	interrupts enabled (for all interrupts)
15	interrupt pending (unmasked)

Table 2: Interface status register (ISR) bits (read-only)

4.2 ICR - Interface Control Register

Bits	Meaning
2..7	Write-only interrupt vector. Level is patched on card with links.
8	own channel bit 0
9	own channel bit 1
10	Online
14	interrupt enable (0 disable, 1 enable).

Table 3: Interface control register (ICR) bits (write-only).

Table 3 shows the interface control register bit assignment. Any value can be written to the control register, but not all of the bit positions are significant.

Bits 2 to 7 contain the interrupt vector base address. The value written here is used as the high six bits of the vector for the eight-bit VME vectored interrupt mechanism. Note that there is no way to read the interrupt vector base register over the VME bus.

Bits 8 and 9 enable the host to control the station's own channel number. The own channel number may be freely set by the station and changed at anytime. A suitable time to select and set the own channel is when the first reception VCI is set up (by creating a map entry). The own channel value may require up to about 200 ms before it is propagated (by the monitor module) to all of the boards that make up the station.

Writing to bit 10 enables the host to take the station on or off-line. The station can be taken on and off line freely by writing the online bit, provided the front panel switch 'online/offline' is in the online position. The function is the AND of Bit 10 and the value from the switch. The flag in the status register (ISR) shows the resultant of the AND operation. When online, the station operates normally. When offline, the station will not send or receive from the ring, but all of the host operations remain supported.

Name	Address	Operations allowed
ISR (Status)	EDE0.0004	read only D16
ICR (Control)	EDE0.0000	write only D16
TXsynch	EDE0.0100	write only D16
RXsynch	EDE0.0200	write only D16
RESET	EDE0.0300	write only D16
DMATX0	EDE0.0440	write only D32
DMATX1	EDE0.0450	write only D32
DMATX2	EDE0.0460	write only D32
DMATX3	EDE0.0470	write only D32
DMARX	EDE0.04C0	write only D32
LASTBYTE	EDE0.0502	read only d16
RXfifo	EDE2.8004	read only D16/D32
TX0fifo	EDE2.8000	write only D16/D32
TX1fifo	EDE2.8100	write only D16/D32
TX2fifo	EDE2.8200	write only D16/D32
TX3fifo	EDE2.8300	write only D16/D32
MapAccess	EDE4.0000	read/write D16
to	EDE5.FFFE	
Direct access	EDE6.0000	read/write D16/D32
to buffers	EDE7.FFFE	

Table 1: V1DMA top-level programming model.

4 Interface registers

Table 1 shows the programming model and register addresses assuming a base address of EDE0.0000.

4.1 ISR - Interface Status Register

Table 2 shows the bit assignments of the read-only status register. Bit positions for which no function is shown may be used in future for monitoring additional status; their values should not be relied upon. The low five bits indicate the status of the five FIFO queues maintained by the station. They are zero if corresponding queue is empty and one if not empty (known as the 'logged' state, short for 'backlogged').

Bits 6 and 7 present the reason for the most recently generated interrupt. See section 5 for a full description of the interrupt mechanism. Bits 8 and 9 give the two-bit own channel number for the receive side of the station.

Bit 10 is the 'online' flag. When set, the station is online and enabled for receive and transmit. This is the logical AND of the front panel switch and the host writeable flag in the ICR (bit 10).

Bit 11 is the 'ready' flag which indicates that the ring has slots on it. The ready flag is set whenever a physcial layer frame enters the station on the fibre and is cleared by a timer if there have been no frames for 16 microseconds. The 'ready' LED on the slow board reflects the status of this flag.

Bits 12 and 13 are wired to one and zero in order for test software to establish the presence of the interface. Bit 14 is the interrupt mask. When set, interrupts are enabled. Bit 15 indicates that an interrupt is pending, regardless of the state of bit 14.

3.2 Endianality and order of transmission.

As is the case with the Cambridge Fast Ring, the VCI (destination address) sits in the first 16 bits of the cell. These are the low 16 bits of the first 32 bit word of the cell. [1]

For D16 operation, a standard V1DMA board assumes a big-endian machine such as a 68K (this is not meaningful for D32 transfer). The VCI field sits in the first 16 bit word of the cell. This contains the low 16 bits of the first 32 bit word of the cell. Therefore, using D16 writes, the VCI is written in the second cycle. Little-endian processors can be supported with an alternate set of PALs.

When using a big-endian machine, (like the 68030), with D16 transfers, the high order half-word is written or read over VME bus before the low order, but normally D32 cycles should be used when possible.

3.3 The Five FIFO Queues of Cells

The V1DMA station contains five separate queues of cells. These are each implemented as a simple circular buffer of 256 cell slots.[2] One queue contains received cells and the others contain cells queued for respective transmission on each of the four ring channels. A cell must be transmitted on the channel which matches the 'own' channel assigned to the receiving station.

In order to transmit, it is sufficient to write cells into the fifo. Nine 32-bit writes or eighteen 16-bit writes are required per cell. The V1DMA stations do not inform the host if a transmit queue is overflowing. This is event jolly unlikely at the moment owing to the low loads and slow hosts.

For reception, D32 words and D16 half-words may be read from the receive queue in the order that they were written. Again, with V1DMA there is no indication of receive queue over-run.

For DMA reception, the cell header word should first be read from the RXfifo location, then the physical address of the first of eight 32 bit words should be written into the DMARX location.

For DMA transmit, the cell header word must be written by programmed IO and then a DMA transfer of the 8-word payload commenced by writing to the DMATXn location, where n is the correct channel number.

The DMA request priority (0 through 3) is set with links on the slow board. J16 is bus request 0. J17 is bus request 1. J18 is bus request 2. J19 is bus request 3. Also, the bus grant links block containing LK1 through LK4 must be set. LK1 is for bus request 0. LK2 is for bus request 1. LK3 is for bus request 2. LK4 is for bus request 3. For example, the standard setting is at bus request 2, where J18 is fitted, LK3 has two links fitted to its outer pairs and links LK1, LK2 and LK4 have links between their middle two pins (of four).

---

[1] People sometimes ask what is the physical order of transmission of bits along the fibre. The Backbone Ring follows a strict policy of least-significant-first transmission: i.e. bit 0 of byte 0 of channel 0 is sent first. This is of no importance at the level of the host interface.

[2] This is one of the things which is changed on the V1C interfaces, which use linked lists of cells in their buffers.

Type	VCI	Data Field	Response
1	16	256+16 = 272	1

Figure 4: Backbone Ring Cell Format.

- Reset switch position - momentary reset switch for telemetry CPU.
- Normal switch position - normal mode
- Disable monitor switch position - not used.
- Transmit data - copper connection to same-named port on Fast board.
- Fibre out - 100 microwatt fibre output. Do not look directly in to it at close range.

The Fast board requires a -5 volt rail to be applied to pins 1a and 1c of the J2 connector. Current is 1.5 amps.

2 VME bus interface details

2.1 Base Address

The default base address of the board in VME address space is 0xEDE0.0000 and this is assumed throughout this document. An alternate address of 0xEDF0.0000 is also available for occasions when two V1DMA stations are plugged into the same VME backplane. The alternate base is selected with link 5 on the Slow board, which should be opened for the alternate address. Address modifiers between 00 through 0F are responded to for A32 bus cycles.

Address modifiers between 30 through 3F are responded to for A24 bus cycles. The default base address then becomes E0.0000 and the alternate F0.0000.

2.2 Operation Size

The V1DMA interfaces support both D32 and D16 transfers, according to the VME long-word signal. When making access to 32 bit registers within the device using a pair of D16 transfers, it is important that both D16 transfers are completed. An incomplete transfer may upset a subsequent D16 operation in the same direction (read or write). It is, however, acceptable to interleave D16 read and write operations in any order. Any unknown state in the interface can be cleared with the RX or TX synch commands, depending on the direction of transfer.

3 Station Cell Queues and Host Access to them

3.1 Cell Format

Figure 4 shows the format of a Backbone Ring cell. A cell contains a 16 bit VCI and a 272 bit payload. The first 16 bits of the payload are generally used for link-level protocols and so 256 bits remain for data. The V1DMA interfaces do not offer access to the 'type' and 'response' flags of the cell (although the bits are present on the network).

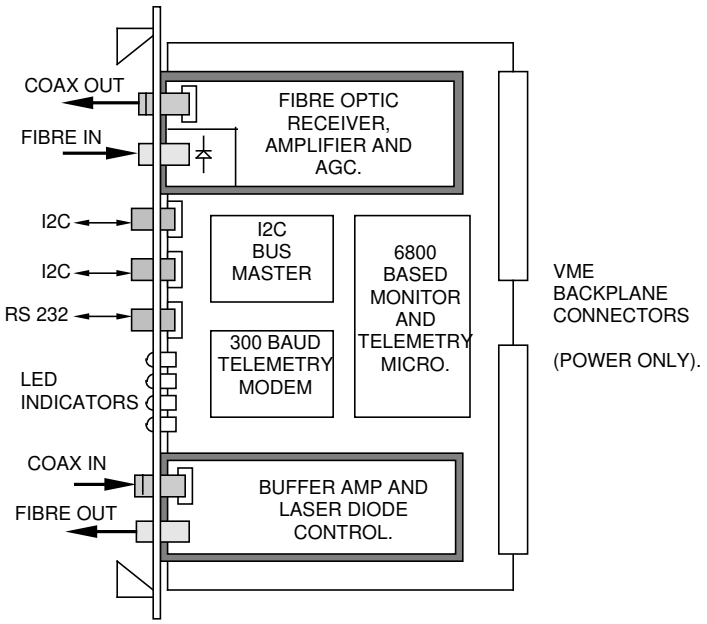

Figure 3: Layout diagram of the telemetry board 2.2. connection.

- Synch Error led - Station is out of synchronisation with fibre bit stream.
- CRC OK led - The CRC of the last PHY frame was ok.
- Bit Error led - fibre reception line errors happening.
- Transmit Data - Coax link to same-named connector on Telemetry board.
- Receive Data - Another coax link to same-named connector on Telemetry board.

1.3 Telemetry Board Controls and LEDs

- Light led - on if sufficient light is being received down the fibre.
- Fibre in port - receive fibre from previous station.
- Received Data socket - Coax link to same-named connector on Fast board.
- Telem 1 socket - I2C bus connection to Fast board.
- Telem 2 socket - spare I2C bus connection - not used.
- RS232 socket - DECNET (R) style terminal connection 9600 Baud.
- Telemetry in led - on during received telemetry frame.
- Telemetry ring led - on if telemetry finds a fully connected ring (can be up to 80 seconds out of date).
- Jolly Good led - on if monitor station reports ring fully ok (will be up to about 7 seconds out of date on non-monitor stations).
- Active led - flashed by telemetry CPU to indicate not crashed.

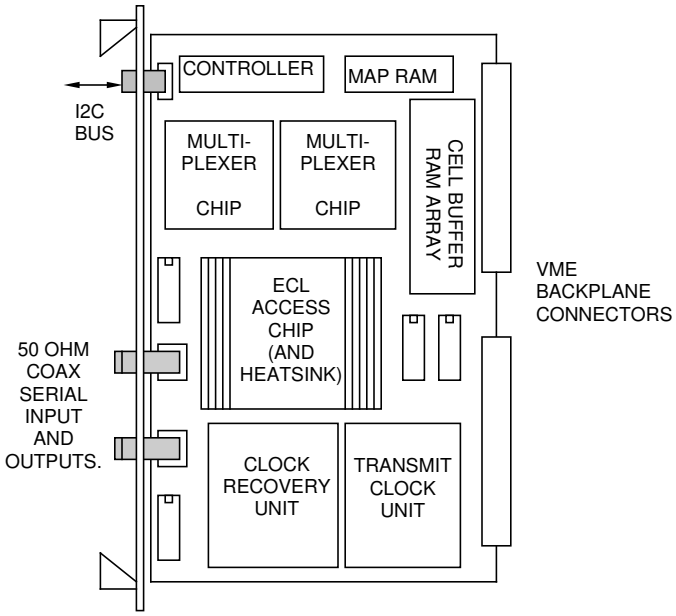

Figure 2: Layout diagram of the fast board 2.2.

1.1 Slow Board Controls and LEDs

- Bus active led - indicates that board is DMA bus master.
- Ready led - indicates that slots are going around the ring.
- Interrupt led - an interrupt is pending and not yet serviced.
- RxLogged led - cells are awaiting in the receiver fifo.
- Desire 0 through 3 leds - on when cells are awaiting in respective transmit fifos.
- Transmit led - on while cell transmission onto ring is in progress.
- Receive led - on while cell reception from ring is in progress.
- Offline switch position - disable all cell reception and transmission from ring.
- Online switch position - normal mode.
- False switch position - generate false traffic on channel 1.

1.2 Fast Board Controls and LEDs

- Telem In socket - I2C bus connection to Telemetry board.
- Telem Out socket - wired in parallel with Telem in for daisy-chaining.
- Telemetry OK led - flashed by fast board CPU to indicate not crashed.
- Master clock led - on if station is enabled as master clock (normally implies monitor station).
- CTRL0 CTRL1 leds - used for debugging.

Backbone Ring (V1DMA) Users' Manual

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February 19, 1992

This users' manual describes the V1DMA Backbone Ring stations. It assumes that the reader is familiar with the Backbone Ring architecture. The Backbone Ring V1DMA stations operate at 512 MHz and are of the half-duplex, single channel type. They support the A32, A24, D16 and D32 VME bus options. The V1DMA stations do not support the hardware retransmission, hardware response mechanism, the type mechanism and multiple priority queues of the basic Backbone Ring architecture [1].

1 Hardware

Figure 1 is a block diagram of the V1DMA stations described in this document. Each station consists of a set of three double-height, extended-depth eurocards:

1. **Fast Board 2.2**, containing the master clock and clock recovery daughter boards, the ring access chip set, the receive address bit map and the cell buffer memory. It is shown in Figure 2.

2. **Slow Board 2.1**, containing the station protocol control logic and buffer address generator.

3. **Telemetry Board 2.2**, containing the optical transmitter and receiver modules, an 8 bit microprocessor, and a 9600 baud serial terminal interface. It is shown in Figure 3.

Two coax cables and an I2C serial bus link the telemetry board to the fast board.

The fast board is connected to the slow board using the 64 user-defined pins on the VME backplane. These pins are jumpered across the reverse side of the VME backplane at the appropriate sockets. This connection provides the address and control inputs for the buffer rams and also carries a number of dedicated signals which control the cycle-by-cycle operation of the station. It also carries an extension of the I2C bus.

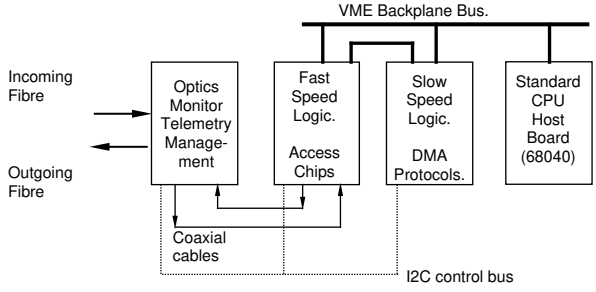

Figure 1: The V1DMA Backbone Ring stations, showing the three circuit boards and a processor card.