ATM Camera V1

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The V1 ATM Camera was built during Spring '92 as a part II Tripos project. Only the original prototype of wire wrap construction exists. A more detailed technical description appears in the Part II dissertation, available from the Computer Laboratory library. Plans are afoot to build a 2nd version, with enhancements like on-board hardware compression and resizing etc.

The ATM Camera takes RGB analogue video and produces an ATM cell stream for a Fairisle switch fabric. The picture details and output routeing information are set by sending a configuration cell to the device on a special VCI. Two modes of operation are available, stream mode and request mode. The former results in every frame of video being sent, whereas the latter sends just a single field/frame on request. Sending a configuration cell provides the request, and is used turn stream mode on and off.

1 LEDs and connectors

There are three LEDs on the 'front panel'. They are used as follows:

Colour	Use
Green	Both Xilinx chips initialised OK. Should always be on.
Yellow	'Locked on' to video sync signal
Red	Transmit - cells are being sent to the fabric.

If the yellow LED does not come on it usually indicates that either a) no configuration cell has been received, b) the configuration cell told the Camera to extract sync info from the wrong input signal, or c) the actual video camera is disconnected / switched off.

There are 4 BNC connectors on the board. Descending from the top of the board they are Composite Sync, Red, Green and finally, Blue.

The prototype has just a single fabric connector, so must be inserted into the bottom backplane in a 16x16 switch.

2 Video input

The ATM Camera's video input section can have two sets of video inputs connected to it, the input actually digitised is selectable by the configuration cell sent to the camera. The second input set is accessable via the 5 way header next to the ADC. The inputs are 'standard' analogue RGB, ie. AC coupled, 0.7V pk-pk video with an optional 0.3V sync

signature. The device contains all the necessary circuitry to DC restore the signal, based on the horizontal blanking period. A separate composite sync input is provided should sync not be present on red, green or blue. The input to extract sync from is selectable via the configuration cell. The ATM Camera would normally receive its RGB signal from a colour decoder eg. the PAL decoder built by Nick Batterham, but a monochrome picture may be obtained by connecting a composite video signal to one of the colour inputs (by convention this is usually green), and selecting 'extract sync from green'. It would be normal to set the rest of the ATM Camera configuration for 8 bit monochrome mode also.

All the inputs may be selectively 75Ω terminated by the jumpers installed next to each BNC connector. Care should be taken to ensure that the video inputs never exceed 2V pk-pk as this may permanently damage the Brooktree ADC.

3 Cell stream format

The V1 ATM Camera generates a cell stream that is line orientated. A line consists of a single control cell followed by a number of data cells. The 48 byte payloads of the data cells consist of raw pixel data with no further overhead. The control cell indicates the frame and line number, whether the field is odd or even, and an error bit. Should the ATM Camera receive NACKs from the fabric, it will retry the cell. It operates a policy of always trying to send the freshest line, so, should the ADC finish sampling a new line before the previous one has been fully sent, the unsent portion will be dropped, and the error bit set in the control cell of the new line. This provides an extra check over the SAR1a information included in the header of each cell. The frame count is simply incremented whenever a frame is requested (or every frame in stream mode). It is intended to be used to identify to which frame a line belongs, rather than as a timestamp. The V2 ATM Camera may contain a separate 1MHz oscillator for time stamping purposes.

The control cell format is as follows:

Octet	Use
0	low eight bits of line number
1	bit 0,1 contain the upper line number bits bit 6 is set for an odd frame, clear for even bit 7 is set if the last line was truncated
2	8 bit frame counter

The control cell is marked by having the 'Frame Start' bit set in the SAR1a format FAS field. The last data cell will have the 'Frame End' bit set. The sequence field descends to one on a per line basis, and assemble field increments every line.

The data cells contain either sixteen 24 bit pixel values or forty-eight, 8 bit pixels, depending on whether the Camera is in 24 or 8 bit mode.

4 Picture size and position

The size, sample rate, and position in the frame of the picture can be set via the control cell. The horizontal sampling frequency can be set by integer division of an oscillator,

usually a 50MHz crystal. Division by 2n (where $1 \leq n < 256$) is possible. With a 50MHz crystal this yields a number of useful frequencies, e.g. 12.5, 8.3, 6.3, 5.0, 4.2 MHz. The board locks this divided pixel clock to the horizontal sync derived from the composite sync input. This locking eliminates the 'jaggedness' that would appear on vertical lines if phase drift was allowed to occur.

The picture size and position in the frame are set via a number of parameters in the configuration cell. The vertical delay parameter sets the number of lines from the end of VSync before sampling commences. For a 'full frame' grab, this will typically be 15. The vertical count parameter specifies the number of lines to be sent. There is a vertical skip parameter that is a bit field that is rotated one bit position at the start of every line. If the bit is set, the line is sampled, otherwise it is skipped. The vertical count is decremented only when a line is actually sent. Thus, the vertical count divided by the ratio of 1s to 0s in the VSkip field determines the number of video lines the picture is sampled over. A PAL format picture contains 288 active picture lines per field. The total number of lines per field is 312.5. The half line is due to interlace requirements. The ATM Camera has two sets of the three vertical parameters, one used during odd fields, the other during even.

The horizontal size and position are set by similar parameters to the vertical ones. There is a horizontal delay, which is the number of pixel clocks before sampling commences. It should be noted that this time period is dependent on the current oscillator divide frequency set for the pixel clock. The number of pixels sampled horizontally is determined by the 'cells per line' field. Each cell contains either 16 or 48 pixels, depending on whether 8 or 24 bit mode is selected. 'Cells per line' includes the control cell sent at the start of each line, so the number of pixels sampled will be either 16.(x-1) or 48.(x-1) depending on the mode. There is also a horizontal skip parameter. This provides additional control over the sampling frequency, rotating one bit position each pixel clock, and only sampling if the value contains a 1 in the lsb.

These parameters can be used to create correct aspect ratio, full-frame pictures of a number of sizes. Alternatively, values can be chosen to grab only part of the full frame. This might be used to grab the part of the frame that currently contains the area of interest eg. a person's head as they move around in front of the camera during a video conference. A number of configuration examples occur at the end of this document.

The camera does not error check any values passed to it. This means it is quite possible to give the camera parameters that cause it to try to grab a frame whose boundaries exceed the active picture part of the video signal. The likely result of this is that the Camera will send no data back. This is most likely to occur if too many cells are requested for a given pixel clock rate. This may cause HSync to occur before the Camera has finished grabbing the current line. No data will be sent back and the red TX LED will not flash on.

5 ADC Control

The ADC has a number of registers that are initialised with values sent in the configuration cell. The most important is the control register. Rather than giving the gory details of what each bit does (read the Brooktree B253 book), here are some useful values :

Value	Use
2Ch	8 bit monochrome on the Green BNC input, sync on Green
28h	8 bit 3:3:2 colour, sync on green
68h	8 bit 3:3:2 colour, separate sync
20h	24 bit colour, sync on Green
60h	24 bit colour, separate sync

The ADC allows the top and bottom reference voltages to be set for each of R,G and B. These voltages apply to the DC restored signal, where the horizontal blanking period will be clamped to 0V. The voltage is set using the formula n x 4.75mV. Between the top and bottom reference values, the ADC provides a linear 8 bit output. Values outside the thresholds are clamped. Varying of these voltages allows brightness, contrast and colour balance compensation. For example, decreasing all the top thresholds will brighten the picture. Narrowing the gap between the top and bottom thresholds will increase contrast. Colour temperature hues can be corrected by varying the relative brightness of R, G and B. For indoor lighting, the blue threshold may be raised slightly to give a more yellow picture. All six reference values are set via the configuration cell.

6 Configuration Cells

The ATM Camera needs just one type of configuration cell, which it looks for on VCI 255.254. Cells sent on other VCIs are ACKed but ignored. This was done so that the port on the switch the ATM Camera is plugged in to can be investigated. By sending a configuration cell requesting a single line of data at one 'cell per line', the investigating device will receive one cell back from the Camera indicating its presence. This mechanism is not particularly aesthetic, but it was felt important to keep the Camera a 'dumb' device. It should be noted that the Camera only sends cells if it is successfully extracting a sync signal from one of its inputs (thus the yellow LED is on). This means the ATM Camera may not reply to an investigative cell if the actual video Camera is switched off, not connected etc. Once a standard for DAN device investigation is determined, the v2 camera will implement it.

The first byte in the configuration cell is the Control Register value. Four bits of this octet are used:

Bit	Name	Use
0	Steam Mode	1 = on, 0 = off
1	Single Odd	1 = request single frame
2	Single Even	1 = request single frame
3-6	Reserved	should be zero
7	Colour mode	1 = 8 bit mode (mono or 3:3:2), 0 = 24 bit mode

The 48 byte payload of the configuration cell is used as follows:

Octet	Name	Use
00h	Control Reg	See separate table.
01h	Cell Count	Number of cells to send a line including Control cell.
02h	V Skip Odd	Bit pattern used to sub sample lines during odd fields.
03h	V Skip Even	Bit pattern used to sub sample lines during even fields.
04h	V Count Odd Low	Number of odd lines to send, least sig. byte.
05h	V Count Odd High	Number of odd lines to send, most sig. byte.
06h	V Count Even Low	Number of even lines to send, least sig. byte.
07h	V Count Even High	Number of even lines to send, most sig. byte.
08h	H Delay	Horizontal delay before grab window, in pixels.
09h	H Skip Low	l.s.b. of bit pattern used for horizontal sub-sampling.
0Ah	H Skip High	m.s.b. of bit pattern used for horizontal sub-sampling.
0Bh	V Delay	Vertical delay in lines from VSync before grab window.
0Ch	Route Byte 1	Fabric routeing byte to be used for output cells.
0Dh	Route Byte 2	Port Controller route byte to be used for output cells.
0Eh	VCI 1	1st VCI byte for output cells.
0Fh	VCI 2	2nd VCI byte for output cells.
10h	ADC Control Reg	See separate table for details.
11h	Dot Clock Divide	Set pixel clock to 50Mhz / 2(n+1).
12h	ADC Red Top	Set ADC red top threshold to n x 4.75mV.
13h	Reserved	Zero.
14h	ADC Red Bottom	Set ADC red bottom threshold to n x 4.75mV.
15h	Reserved	Zero.
16h	ADC Green Top	Set ADC green top threshold to n x 4.75mV.
17h	Reserved	Zero.
18h	ADC Green Bottom	Set ADC green bottom threshold to n x 4.75mV.
19h	Reserved	Zero.
1Ah	ADC Blue Top	Set ADC blue top threshold to n x 4.75mV.
1Bh	Reserved	Zero.
1Ch	ADC Blue Bottom	Set ADC blue bottom threshold to n x 4.75mV.
1D-2Fh	Reserved	Zero.

It should be noted that the Cell Count indirectly sets the number of pixels in a line. E.g. Asking for 9 cells will give you 1 control cell plus 8 data cells. In 8bit mode, this is 8x48 = 384 pixels.

7 Software

Software exists to demonstrate the Camera in a number of configurations. The original software used an FPC2 plugged in to the same backplane as the Camera. The FPC2 was running a special Wanda kernel to assemble a line's worth of cells into a MSNL block and forward it across the Ethernet to a DEC Station running code to assemble a picture.

The UNIX end of the software can be found in /usr/groups/fairisle/iap10/xfg. There are two programs, xcam and camclient. 'xcam' produces a continuously updated video window, whereas camclient produces a .ppm file as its output. The xcam program achieved about 4 frames per second of 160x120 video across the Ethernet on a good day.

The camclient program built up a high resolution image from a number of sub-sampled

lower resolution ones. This was necessary to avoid filling the FPC2's 2000 cell input buffer.

The latest software being developed by Eoin Hyden uses a Fairisle TAXI link interface to transport the video to a YES V2 board fitted to a DS5000/25. The DEC Station runs Wanda with a user process to display the video. Much higher transfer rates are possible. In 8 bit colour mode, 12 frames per second of 384x288 video are possible. The full 50Hz frame rate can be achieved with smaller images.

The data rate involved in doing the larger images peaks at about 60Mbits/s over a line.

8 Example Configuration

A PAL video field consists of 312.5 lines, of which 288 are active picture. The first active picture line is around line 12 from VSync. Horizontally, a line lasts 64μs. The active picture part lasts about 52μs, starting about 8μs after HSync. These parameters vary from video source to video source, but are usually a good guide.

To produce a 384x288 image:

1. If we are in 8 bit mode, each cell contains 48 pixels, therefore the number of data cells = 8. Including the control cell, the Cell Count per line will be 9.
2. The 52 μs of active image lasts 384 pixels, therefore, the dot clock frequency needs to be at least 7.4MHz.
3. With a 50MHz oscillator, the closest frequency we can get using the 50MHz/2(n+1) formula is 8.3MHz, where n=2. Note that it is necessary to go for the next highest frequency to avoid going outside the active video area, possibly resulting in the Camera not responding.
4. For an 8.3Mhz clock, the 8μs horizontal delay lasts around 66 pixels.
5. Since we are grabbing all 288 lines in the field, all the VSkip values will be 0xFF.
6. We to not need to do any sub-sampling horizontally, so HSkip = 0xFFFF.

This yields:

Cell Count = 9, Dot Clock Divide = 2, VSkip Even = VSkip Odd = 0xFF,
VCount Even = VCount Odd = 288, VDelay = 12, HDelay = 66, HSkip = 0xFFFF.

Based on this, a 192 x 144 image could be produced simply by changing:

Cell Count = 5, VSkip Even = VSkip Odd = 0x55, VCount Even = VCount Odd = 144, HSkip = 0xAAAA.

Note that VDelay and HDelay don't change despite the skip values. This is because the skip values do not take effect untill after the delay periods have expired (during the sampling window).

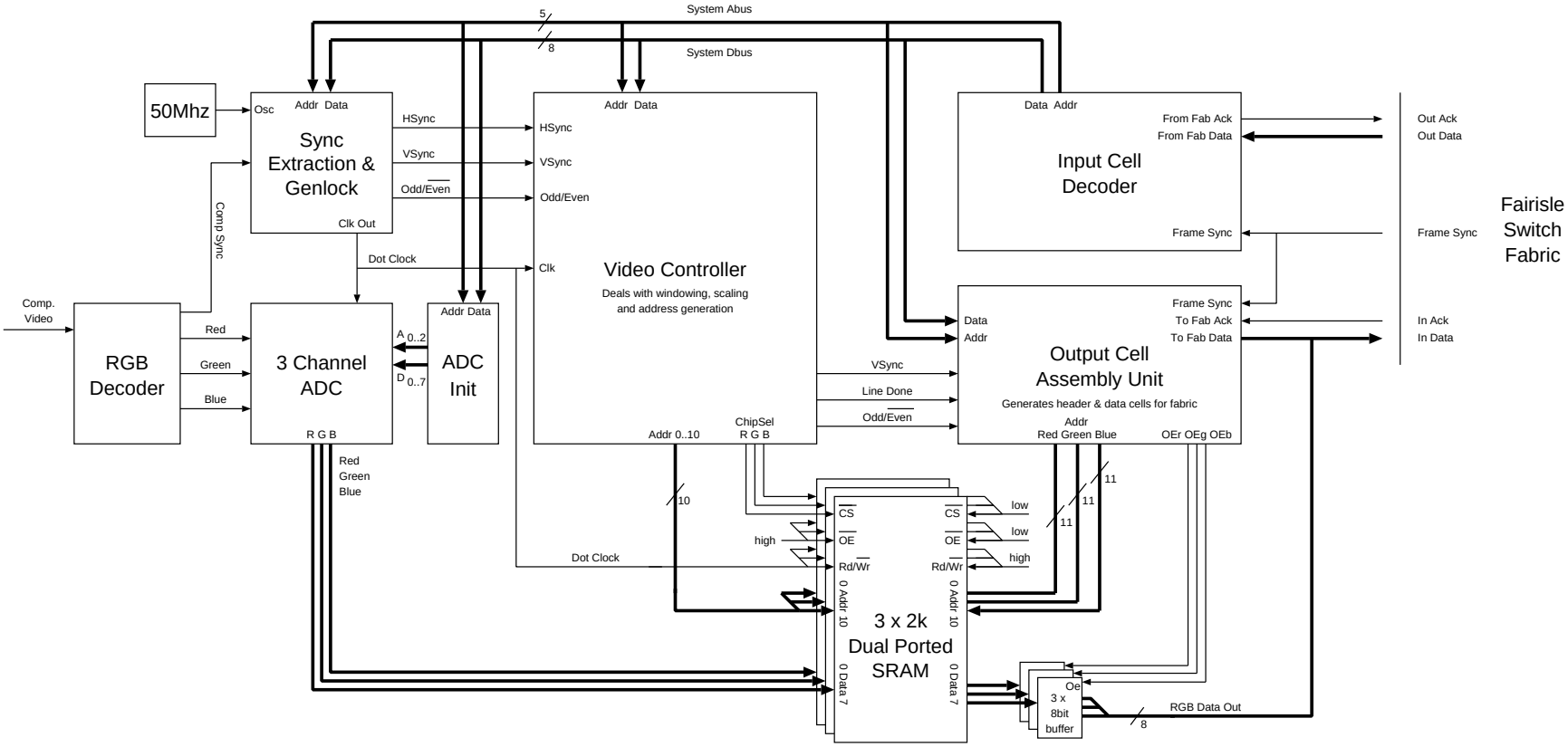

fig 1 - ATM Camera architectural schematic