

# Temporal Logic and Model Checking

- ▶ **Model**
    - ▶ mathematical structure extracted from hardware or software
  - ▶ **Temporal logic**
    - ▶ provides a language for specifying functional properties
  - ▶ **Model checking**
    - ▶ checks whether a given property holds of a model
- 
- ▶ Model checking is a kind of **static verification**
    - ▶ dynamic verification is simulation (HW) or testing (SW)

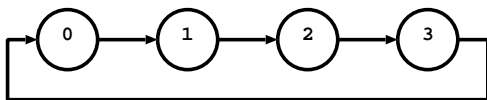
# Models

- ▶ A model is (for now) specified by a pair  $(S, R)$ 
  - ▶  $S$  is a set of *states*
  - ▶  $R$  is a *transition relation*
  
- ▶ Models will get more components later
  - ▶  $(S, R)$  also called a transition system
  
- ▶  $R s s'$  means  $s'$  can be reached from  $s$  in one step
  - ▶ here  $R : S \rightarrow (S \rightarrow \mathbb{B})$  (where  $\mathbb{B} = \{true, false\}$ )
  - ▶ more conventional to have  $R \subseteq S \times S$ , which is equivalent
  - ▶ i.e.  $R_{\text{(this course)}} s s' \Leftrightarrow (s, s') \in R_{\text{(some textbooks)}}$

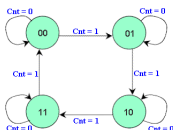
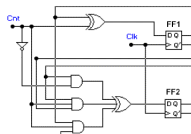
# A simple example model

- ▶ A simple model:  $(\underbrace{\{0, 1, 2, 3\}}_S, \underbrace{\lambda n n'. n' = n+1(\text{mod } 4)}_R)$

- ▶ where “ $\lambda x. \dots x \dots$ ” is the function mapping  $x$  to  $\dots x \dots$
- ▶ so  $R n n' = (n' = n+1(\text{mod } 4))$
- ▶ e.g.  $R 0 1 \wedge R 1 2 \wedge R 2 3 \wedge R 3 0$



- ▶ Might be extracted from:



[Acknowledgement: [http://eelab.usyd.edu.au/digital\\_tutorial/part3/t-diag.htm](http://eelab.usyd.edu.au/digital_tutorial/part3/t-diag.htm)]

## DIV: a software example

- ▶ Perhaps a familiar program:

```
0:  R:=X;
1:  Q:=0;
2:  WHILE Y≤R DO
3:    (R:=R-Y;
4:     Q:=Q+1)
5:
```

- ▶ State  $(pc, x, y, r, q)$

- ▶  $pc \in \{0, 1, 2, 3, 4, 5\}$  program counter
- ▶  $x, y, r, q \in \mathbb{Z}$  are the values of X, Y, R, Q

- ▶ Model  $(S_{DIV}, R_{DIV})$  where:

$$S_{DIV} = [0..5] \times \mathbb{Z} \times \mathbb{Z} \times \mathbb{Z} \times \mathbb{Z} \quad (\text{where } [m..n] = \{m, m+1, \dots, n\})$$

$$\begin{aligned} \forall x y r q. R_{DIV} (0, x, y, r, q) (1, x, y, x, q) & \quad \wedge \\ R_{DIV} (1, x, y, r, q) (2, x, y, r, 0) & \quad \wedge \\ R_{DIV} (2, x, y, r, q) ((\text{if } y \leq r \text{ then } 3 \text{ else } 5), x, y, r, q) & \quad \wedge \\ R_{DIV} (3, x, y, r, q) (4, x, y, (r-y), q) & \quad \wedge \\ R_{DIV} (4, x, y, r, q) (2, x, y, r, (q+1)) & \quad \wedge \end{aligned}$$

- ▶ [Above changed from lecture to make  $R_{DIV}$  partial!]

# Deriving a transition relation from a state machine

- ▶ State machine transition function :  $\delta : Inp \times Mem \rightarrow Mem$ 
  - ▶ *Inp* is a set of inputs
  - ▶ *Mem* is a memory (set of storable values)

- ▶ Model:  $(S_\delta, R_\delta)$  where:

$$S_\delta = Inp \times Mem$$

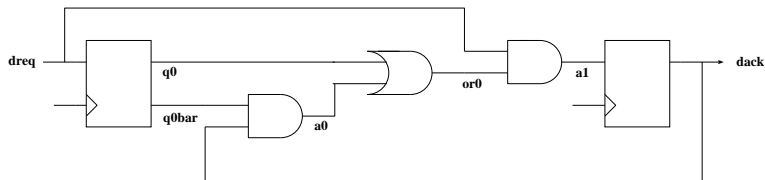
$$R_\delta (i, m) (i', m') = (m' = \delta(i, m))$$

and

- ▶ *i'* arbitrary: determined by environment not by machine
  - ▶ *m'* determined by input and current state of machine
- ▶ Deterministic machine, non-deterministic transition relation
  - ▶ inputs unspecified (determined by environment)
  - ▶ so called “input non-determinism”

## RCV: a state machine specification of a circuit

- ▶ Part of a handshake circuit:



- ▶ Input:  $dreq$ , Memory:  $(q0, dack)$

- ▶ Relationships between Boolean values on wires:

$$\begin{aligned}q0bar &= \neg q0 \\ a0 &= q0bar \wedge dack \\ or0 &= q0 \vee a0 \\ a1 &= dreq \wedge or0\end{aligned}$$

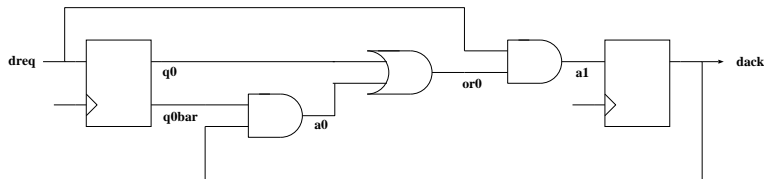
- ▶ State machine:  $\delta_{RCV} : \mathbb{B} \times (\mathbb{B} \times \mathbb{B}) \rightarrow (\mathbb{B} \times \mathbb{B})$

$$\delta_{RCV} \left( \underbrace{dreq}_{Inp}, \underbrace{(q0, dack)}_{Mem} \right) = (dreq, dreq \wedge (q0 \vee (\neg q0 \wedge dack)))$$

- ▶ RTL model – could have lower level model with clock edges

## RCV: a model of the circuit

- ▶ Circuit from previous slide:



- ▶ State represented by a triple of Booleans ( $dreq, q0, dack$ )
- ▶ By De Morgan Law:  $q0 \vee (\neg q0 \wedge dack) = q0 \vee dack$
- ▶ Hence  $\delta_{RCV}$  corresponds to model  $(S_{RCV}, R_{RCV})$  where:

$$S_{RCV} = \mathbb{B} \times \mathbb{B} \times \mathbb{B}$$

$$R_{RCV} (dreq, q0, dack) (dreq', q0', dack') = \\ (q0' = dreq) \wedge (dack' = (dreq \wedge (q0 \vee dack)))$$

[Note: we are identifying  $\mathbb{B} \times \mathbb{B} \times \mathbb{B}$  with  $\mathbb{B} \times (\mathbb{B} \times \mathbb{B})$ ]

## Some comments

- ▶  $R_{RCV}$  is non-deterministic and total
  - ▶  $R_{RCV}(1, 1, 1)(0, 1, 1)$  and  $R_{RCV}(1, 1, 1)(1, 1, 1)$   
(where  $1 = true$  and  $0 = false$ )
  - ▶  $R_{RCV}(dreq, q0, dack)(dreq', dreq, (dreq \wedge (q0 \vee dack)))$
- ▶  $R_{DIV}$  is deterministic and partial
  - ▶ at most one successor state
  - ▶ no successor when  $pc = 5$
- ▶ Non-deterministic models are very common, e.g. from:
  - ▶ asynchronous hardware
  - ▶ parallel software (more than one thread)
- ▶ Can extend any transition relation  $R$  to be total:
$$R_{total} s s' = \text{if } (\exists s''. R s s'') \text{ then } R s s' \text{ else } (s' = s)$$
$$= R s s' \vee (\neg(\exists s''. R s s'') \wedge (s' = s))$$
  - ▶ sometimes totality required  
(e.g. in the book *Model Checking* by Clarke et. al)



# JM1: a non-deterministic software example

- ▶ From Jhala and Majumdar's tutorial:

Thread 1	Thread 2
0: IF LOCK=0 THEN LOCK:=1;	0: IF LOCK=0 THEN LOCK:=1;
1: X:=1;	1: X:=2;
2: IF LOCK=1 THEN LOCK:=0;	2: IF LOCK=1 THEN LOCK:=0;
3:	3:

- ▶ Two program counters, state:  $(pc_1, pc_2, lock, x)$

$$S_{JM1} = [0..3] \times [0..3] \times \mathbb{Z} \times \mathbb{Z}$$

$$\begin{aligned} \forall pc_1 pc_2 lock x. R_{JM1} (0, pc_2, 0, x) & (1, pc_2, 1, x) \quad \wedge \\ R_{JM1} (1, pc_2, lock, x) & (2, pc_2, lock, 1) \quad \wedge \\ R_{JM1} (2, pc_2, 1, x) & (3, pc_2, 0, x) \quad \wedge \\ R_{JM1} (pc_1, 0, 0, x) & (pc_1, 1, 1, x) \quad \wedge \\ R_{JM1} (pc_1, 1, lock, x) & (pc_1, 2, lock, 2) \quad \wedge \\ R_{JM1} (pc_1, 2, 1, x) & (pc_1, 3, 0, x) \end{aligned}$$

- ▶ Not-deterministic:

$$R_{JM1} (0, 0, 0, x) (1, 0, 1, x)$$

$$R_{JM1} (0, 0, 0, x) (0, 1, 1, x)$$

- ▶ Not so obvious that  $R_{JM1}$  is a correct model

# Atomic properties (properties of states)

- ▶ Atomic properties are true or false of individual states
  - ▶ an atomic property  $p$  is a function  $p : S \rightarrow \mathbb{B}$
  - ▶ can also be regarded as a subset of state:  $p \subseteq S$

- ▶ Example atomic properties of  $\text{RCV}$   
(where  $1 = \text{true}$  and  $0 = \text{false}$ )

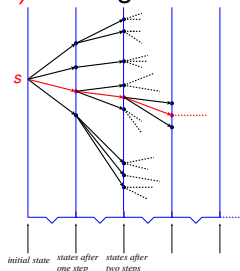
$$\begin{aligned}\text{Dreq}(dreq, q0, dack) &= (dreq = 1) \\ \text{NotQ0}(dreq, q0, dack) &= (q0 = 0) \\ \text{Dack}(dreq, q0, dack) &= (dack = 1) \\ \text{NotDreqAndQ0}(dreq, q0, dack) &= (dreq=0) \wedge (q0=1)\end{aligned}$$

- ▶ Example atomic properties of  $\text{DIV}$

$$\begin{aligned}\text{AtStart}(pc, x, y, r, q) &= (pc = 0) \\ \text{AtEnd}(pc, x, y, r, q) &= (pc = 5) \\ \text{InLoop}(pc, x, y, r, q) &= (pc \in \{3, 4\}) \\ \text{YleqR}(pc, x, y, r, q) &= (y \leq r) \\ \text{Invariant}(pc, x, y, r, q) &= (x = r + (y \times q))\end{aligned}$$

# Model behaviour viewed as a computation tree

- ▶ Atomic properties are true or false of individual states
- ▶ General properties are true or false of whole behaviour
- ▶ Behaviour of  $(S, R)$  starting from  $s \in S$  as a tree:



- ▶ A path is shown in red
- ▶ Properties may look at all paths, or just a single path
  - ▶ CTL: Computation Tree Logic (all paths from a state)
  - ▶ LTL: Linear Temporal Logic (a single path)