

COMPUTER SCIENCE TRIPOS Part IA – 2023 – Paper 2

2 Digital Electronics (ijw24)

(a) D type flip-flops are to be used to implement a synchronous counter having an output sequence 0, 1, 2, 3, 4, 5, 0, ... (decimal).

(i) Determine the next state combinational logic required for the D type flip-flops.

(ii) Show whether or not the counter self-starts. [8 marks]

(b) A finite state machine is represented by the following state table:

Current state ( $Q$ )	Next state ( $Q'$ )				Output ( $Z$ )
	$XY = 00$	$01$	$10$	$11$	
$A$	$A$	$F$	$C$	$B$	0
$B$	$A$	$B$	$D$	$H$	1
$C$	$G$	$B$	$C$	$D$	0
$D$	$C$	$F$	$D$	$D$	1
$E$	$G$	$A$	$E$	$D$	1
$F$	$F$	$F$	$G$	$B$	0
$G$	$G$	$B$	$G$	$E$	0
$H$	$F$	$B$	$E$	$H$	1

(i) Determine the equivalent states using the state equivalence/implication table approach.

(ii) Show the reduced state table. [9 marks]

(c) Consider two D type flip-flops operating in a synchronous configuration. The input of the second flip-flop,  $D_2$ , is connected to the output of a combinational logic block, and one of the inputs to the combinational logic block is connected to the output,  $Q_1$ , of the first flip-flop.

For both flip-flops, the minimum set-up time  $t_{su,min} = 20$  ns, the minimum hold time  $t_{h,min} = 5$  ns, and the maximum propagation delay  $t_{pc,max} = 40$  ns. The maximum propagation delay of the combinational logic block from  $Q_1$  to  $D_2$  is  $t_{pd,max} = 49$  ns.

(i) Determine the maximum clock frequency for this circuit.

(ii) How could this be increased without changing the flip-flops? [3 marks]