6 Introduction to Computer Architecture (swm11)

The Thrupenny Bit FPGA company produces FPGAs with a sea of logic elements (LEs) depicted below (Fig 1) containing 3-bit LUTs (LookUp Tables) and a D flip-flop (DFF). Each LUT can be programmed with any Boolean function of three inputs and one output. The output of the LUT can be sent over the programmable wiring or to the input of the DFF. The DFF has data (D), asynchronous level-sensitive clear and edge triggered clock inputs, and the Q output. The clear input can be used to reset the DFF to zero.

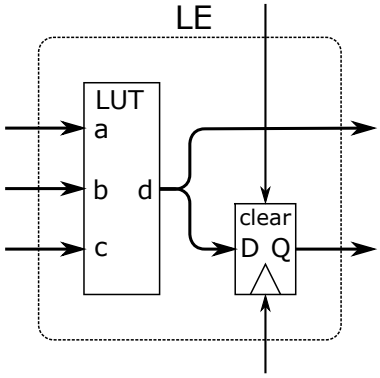

Fig. 1: Thrupenny Bit LE

```
module counter(input  logic       clk,
               input  logic       rst,
               input  logic       enable,
               output logic [2:0] count);

   always_ff @(posedge clk or posedge rst)
     if(rst)
       count <= 0;
     else
       if(enable)
         count <= count+3'd1;
endmodule
```

Fig. 2: SystemVerilog code

(*a*) What is the minimum number of LEs required to implement the `counter` module in Fig. 2 on a Thruppenny Bit FPGA? Provide a detailed rationale. [8 marks]

(*b*) Produce a circuit diagram of your implementation showing how the LEs are wired together. [6 marks]

(*c*) Tabulate the contents of the LUTs for each LE used (i.e. provide a state transition table for each LUT).

[6 marks]