COMPUTER SCIENCE TRIPOS Part II – 2020 – Paper 8

3 Comparative Architectures (rdm34)

(*a*) (*i*) For each of the processors described below outline a possible microarchitecture. Include a labelled block diagram that illustrates the main components of the core pipeline and how they are interconnected. Individual pipeline stages should be shown with a brief description of their contents.

(A) A simple superscalar processor with a short pipeline. It can fetch and issue up to two instructions per cycle and instructions are issued in program order. [4 marks]

(B) A high-performance superscalar processor that supports out-of-order execution. It is able to fetch and issue up to 6 instructions per cycle. It has a deep pipeline and aims to support a high clock frequency. [6 marks]

(*ii*) In practice, the area of these types of processor may differ by a factor of five or more. What contributes to this large difference in area? [5 marks]

(*b*) An indirect branch may have multiple target addresses associated with it. Why is this problematic for a simple Branch Target Buffer (BTB) design? [2 marks]

(*c*) If indirect branches favour a particular branch target, and only infrequently branch to other targets, how might the design of the BTB be optimised? [3 marks]