## 1  Computer Design (SWM)

Consider the following SystemVerilog code containing the module **element**.

```
typedef struct packed {
    logic        v; // valid bit (1=valid, 0=invalid)
    logic [7:0] d; // data
} itemT;

typedef enum {opNone, opRead, opWrite} opT;

function automatic logic swapToggle(itemT a, itemT b);
    return (a.v && !b.v) || (a.d < b.d);
endfunction

module element(
    input           clk,
    input           rst,
    input   opT    op,
    input   itemT dInTop,
    output  itemT dOutTop,
    input   itemT dInBot,
    output  itemT dOutBot);

    itemT    d[1:0];
    logic    swap;

    always_comb
      begin
         dOutTop = d[swap];
         dOutBot = d[!swap];
      end

    always_ff @(posedge clk)
      if(rst)
        begin
           d[0] <= itemT'{d:0, v:0};
           d[1] <= itemT'{d:0, v:0};
           swap <= 0;
        end
      else
        case (op)
          opRead:
            begin
               d[swap] <= dInBot;
               swap <= swap ^ swapToggle(d[!swap],dInBot);
               // Note: ^ is SystemVerilog for XOR
            end
          opWrite:
            begin
               d[!swap] <= dInTop;
               swap <= swap ^ swapToggle(dInTop, d[swap]);
            end
        endcase
endmodule
```

The figure below shows that the **element** module can be instantiated many times over to form a linear structure (technically called a *systolic array*). Valid data (i.e. data with the $v$ bit set) is input on the top left of element 0 during a write operation (op=opWrite). Data is read out from element 0 top right during a read operation (op=opRead). Clock (clk) and reset (rst) signals have been omitted for clarity.
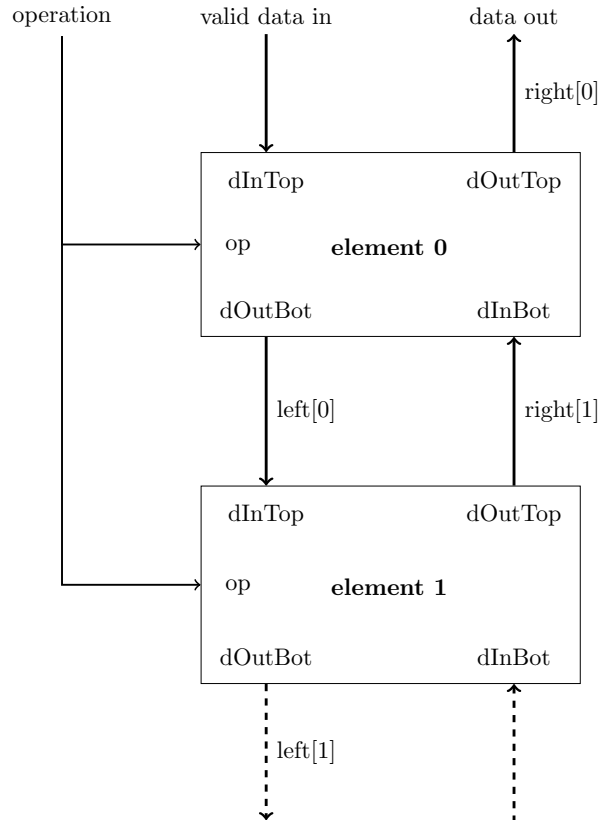


(a) If there are $N$ elements, how many data items (of type itemT) can be stored by this structure? [4 marks]

(b) Four valid data items are written in the sequence: 4, 2, 3, 1. What will be the state of the outputs of element 0 (left[0], right[0]) and element 1 (left[1], right[1]) after each write clock cycle? Clearly enumerate the state changes, including changes to the swap bits. (e.g. via a state transition table) [6 marks]

(c) If there are then four read operations, in what sequence will data be read out? [6 marks]

(d) What function does this systolic array perform and what is its space and time complexity for processing $N$ items by first writing all $N$ items and then reading $N$ items? [4 marks]