2011 Paper 9 Question 10

System-on-Chip Design

(a) What is an *instruction set simulator* (ISS) and what is typically the best way for it to achieve high performance? [2 marks]

(b) What performance bottleneck can typically arise when CPU-intensive software is run on a model of a complete system on chip (SoC)? How can this be avoided and at what costs to modelling accuracy? [4 marks]

(c) What problems can arise when operating system device drivers are run on an ISS that has been optimised according to your answers to parts (a) and (b) above? [4 marks]

(d) Two processors on a SoC have separate address spaces. What does this mean? Describe a simple hardware mechanism for sending non-trivial amounts of data between processors in separate address spaces. Interrupts should be used. [4 marks]

(e) Briefly describe both a *high-level* and a *mid-level* model of your answer to part (d) where the mid-level model requires minimal or no modification to the device driver firmware but is not a net-level model and where the high-level model dispenses with much of the device driver code and many or all of the interrupts. [3 marks each]