2011 Paper 7 Question 4

Comparative Architectures

(*a*) What hardware and software techniques may be used to reduce the number of conflict misses experienced by a direct-mapped cache? [4 marks]

(*b*) How might a hardware prefetcher that is capable of detecting and prefetching non-unit strides be implemented? [4 marks]

(*c*) How can the MESI cache coherency protocol be exploited to ensure that a test-and-set instruction is performed atomically without the need to lock down the bus for multiple cycles? [4 marks]

(*d*) Moore's law predicts we will be able to integrate a very large number of processor cores onto a single chip in the near future. What constraints and challenges may limit our ability to exploit these chip multiprocessors? [8 marks]