2010 Paper 9 Question 12

System-on-Chip Design

(*a*) What is the critical path of a synchronous clock domain and how does it affect performance? [2 marks]

(*b*) Name **two** tools that can be used for locating the critical paths of a system on chip before fabrication. Which is faster or better and why? [4 marks]

(*c*) Explain how pipelining can alter performance. What are its disadvantages? [4 marks]

(*d*) How does pipelining alter the state encoding for a sub-system? [2 marks]

(*e*) Name a tool that can be used to formally check whether a minor design change has altered the behaviour of a subsystem where the state encoding has not been changed. Name another tool for use when the state encoding may have been changed. [2 marks]

(*f*) Using any combination of diagrams, SystemC or RTL, sketch **two** implementations for a design of your choosing that use a different number of flip-flops to achieve the same functionality. Explain whether the reports from each of your two tools from part (*e*) might differ for your two implementations. [6 marks]