2010 Paper 8 Question 5

Comparative Architectures

(*a*) Why is it that clock frequency improvements achieved from increasing the length of a processor's pipeline do not directly improve overall performance? [4 marks]

(*b*) Why might it be advantageous to design a scalar processor with multiple execution pipelines? [5 marks]

(*c*) What advantages does dynamic scheduling offer when compared with static scheduling in a superscalar processor? [5 marks]

(*d*) What has limited our ability to improve the performance of superscalar processors even as fabrication technologies have scaled? [6 marks]