

2009 Paper 5 Question 3

Computer Design

- (a) Why are control-flow machines sensitive to memory access latency? [4 marks]
- (b) What statistical properties of data access patterns do caches exploit to reduce memory access latency? [4 marks]
- (c) What cache line replacement policies might be used for set-associative and direct-mapped caches? [4 marks]
- (d) What are two write-back policies for a cache? [4 marks]
- (e) What does a snoopy cache do in a dual-core machine? [4 marks]