2007 Paper 13 Question 2

Computer Design

instruction fetch	decode and register fetch	execute	memory access	write back

With reference to the pipeline above:

(*a*) What is a *control hazard* and how can it be dealt with? [4 marks]

(*b*) What are *data hazards* and how can they be eliminated? [4 marks]

(*c*) A branch could be executed in either the decode or the execute stages. Assuming that branch prediction and branch delay slots are not used, how many bubbles would be introduced into the pipeline in either case? [4 marks]

(*d*) If the memory access results in a cache miss, what happens to the pipeline? [4 marks]

(*e*) For arithmetic operations the result is available after the execute stage. These results could be written directly to the register file during the memory access stage, but what would be the disadvantages of doing so? [4 marks]