2005 Paper 5 Question 2

Computer Design

(*a*) What is the difference between a *control hazard* and a *data hazard*? [4 marks]

(*b*) How are data and control hazards handled for the following two processors with their respective pipelines?

The N-105 processor pipeline:

instruction fetch	register fetch, decode, execute memory access and write back

The ARM9 processor pipeline:

instruction fetch	decode	execute	memory access	write back

[8 marks]

(*c*) If a load instruction causes a cache miss, what impact does it have on the pipeline? [3 marks]

(*d*) What is the structure of a TLB (Translation Lookaside Buffer)? [2 marks]

(*e*) What impact does a TLB miss have on the pipeline? [3 marks]